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GC101/GC102

T-49-17-01

12/16MHz PC/AT Compatible Chip Set

Features

- Highly Integrated PC/AT Compatible Three Chip Set.
- Supports up to 4Meg DRAM using 1Mbit or 256k devices.
- Available in 16MHz and 12MHz versions.
- Designed in HCMOS for high speed and low power consumption.
- All 'Megacells' are full implementations of standard devices.
- Available as cores for customization in high volume applications.

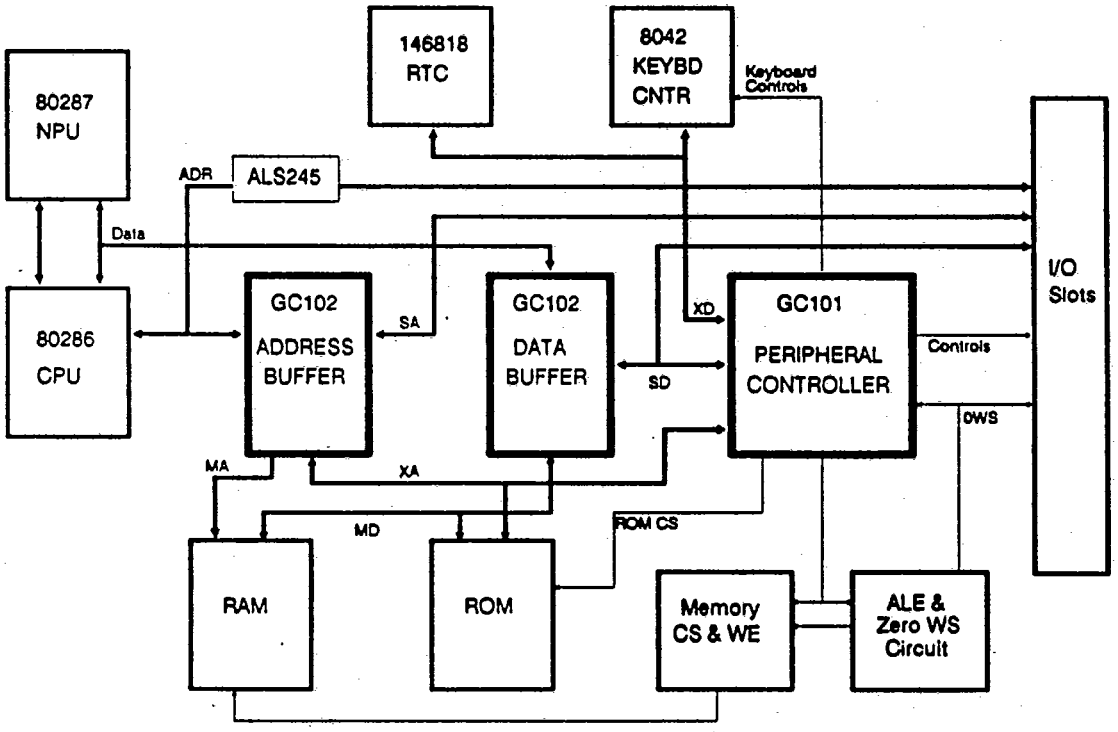
Description

The GC101/GC102 is a fully IBM PC/AT compatible chip set supporting the 80286 CPU at clock speeds up to 16MHz. This highly integrated three chip solution features high performance, low power consumption, low board space requirements, high reliability, and low cost. A fully PC/AT compatible system may be implemented with this chip set, the CPU, Keyboard Controller, RTC and 7 other devices plus memory. This chip set supports 256K and 1 Mbit DRAMs in configurations up to 4 megabytes at zero or one wait state. Zero wait state operations is supported up to 12MHz and one wait at up to 16MHz.

The GC101 performs CPU and Peripheral support functions including that of DMA Controllers, a Memory Mapper, Timers, Counters, Interrupt Controllers, a Bus Controller, and their supporting circuitry. This device is packaged in a 160 pin flat pack.

The GC102 may be configured as either an Address Buffer or Data Buffer by strapping one pin high or low. This chip replaces address buffers, data transceivers, memory drivers, parity generators and supporting circuitry. This device is packaged in an 84 pin PLCC.

System Board Block Diagram



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GC101/GC102

GC101 Peripheral Controller Functional Description

The GC101 Peripheral Controller chip is the heart of the three chip system and forms most of the control circuits and "glue" logic of the AT architecture in a single CMOS VLSI chip. In this device, an 82284 megafunction (MF) generates PROCCLK, /READY and RESET signals for use by the system. MF82288 provides all the CPU I/O command signals for memory, peripherals, and add on boards. A 9-bit refresh counter is used in the circuit to provide the row address of the memory during refresh. MF74612 outputs memory mapping addresses. MF8284 uses a 14.318 MHz input clock to generate an OSC video signal and base clock for the MF8254 timer/counter. The timer is programmed by the CPU and provides signals for system timing, refresh, and speaker tone generation.

Two MF8237s support Direct Memory Access, transferring 8-bit and 16-bit data between memory and I/O devices. Two MF8259s are configured as master/slave and receive interrupt requests from Timer, Keyboard Controller, Real Time Clock, Numeric Processor and up to 11 other sources. The MF8259s issue a signal to the CPU to initiate an interrupt routine. For all peripherals of 8-bit data width, the GC101 provides conversion circuitry from a 16-bit bus to an 8-bit bus, thus maintaining compatibility with an 8088 PC.

The GC101 design encompasses one wait state for memory operation and four wait states for I/O operation. The design includes the option of improving performance by using faster RAM, faster CPU, or by reducing the memory wait state to zero with the addition of external synchronization logic. Designers can configure memory from 256K to 4 Mbytes (or more) by using RSEL0, SEL1 and RSEL2 (see pin listing). There are also select signals to establish chip and system speed. The chip can operate at up to 12/16 MHz in the full commercial temperature range.

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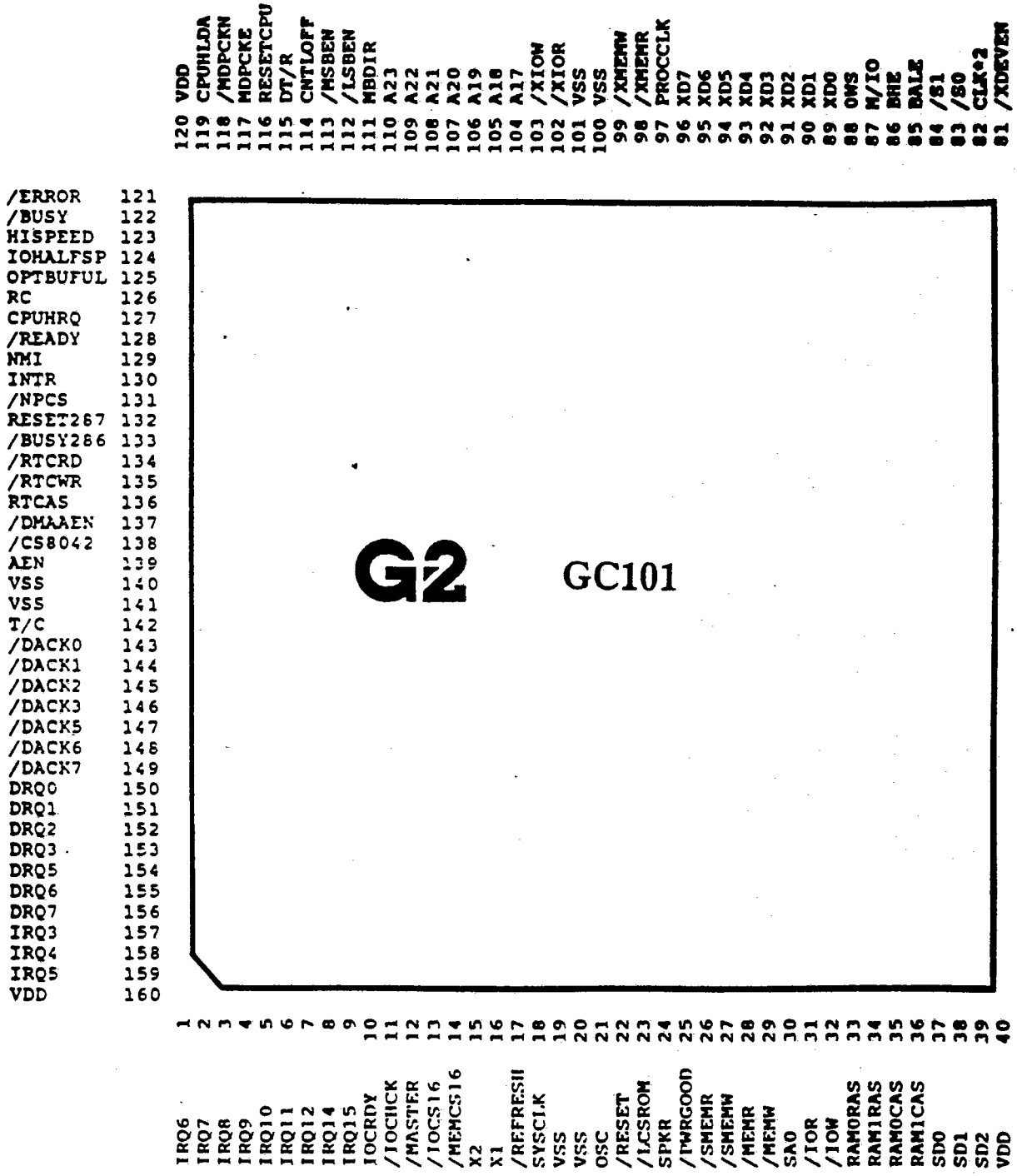
GC101 PIN ASSIGNMENT



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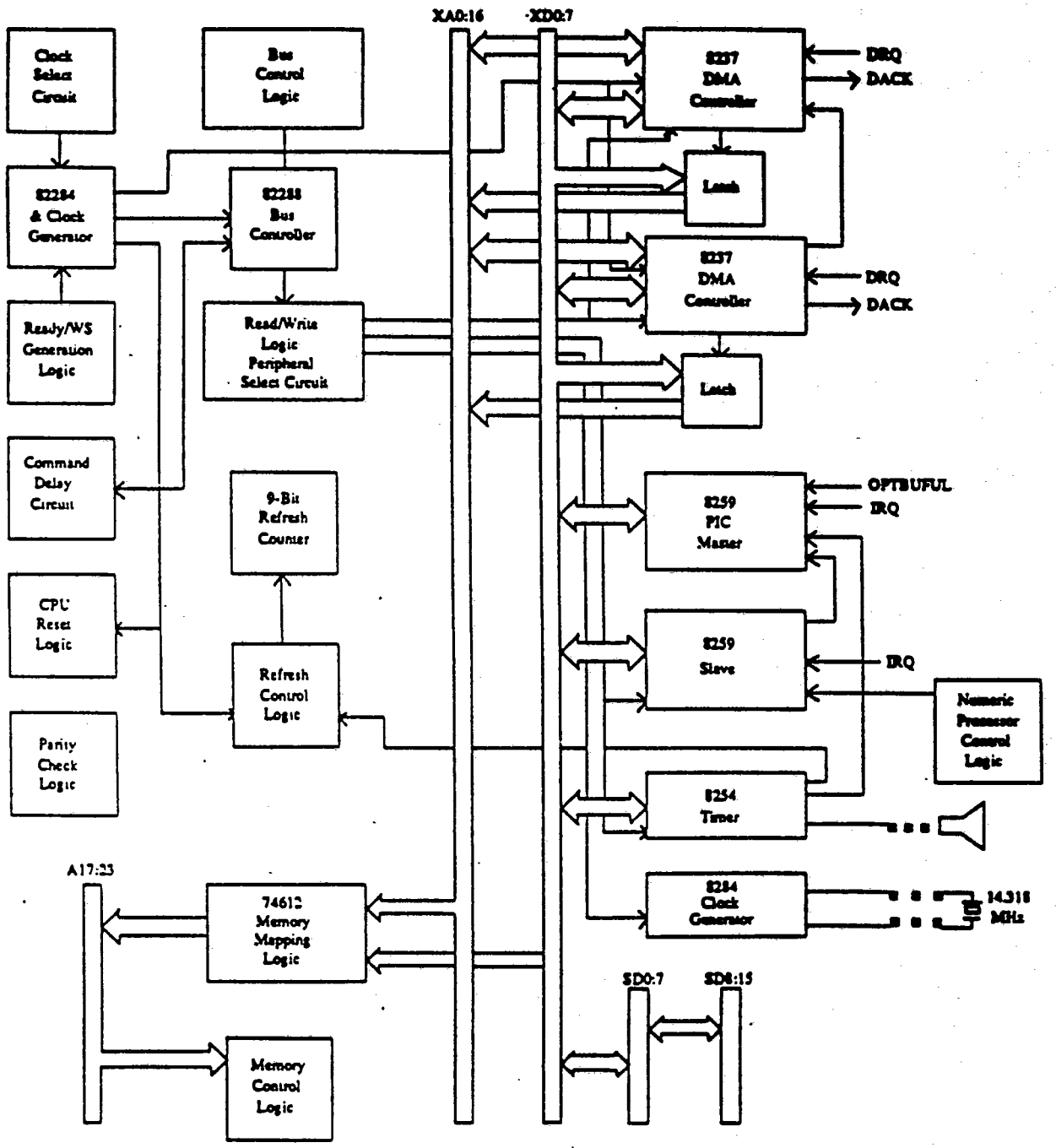
3

GC101 Peripheral Controller Chip Block Diagram



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GC101/GC102

GC101 Peripheral Controller - Pin Description

Pin Symbol	Pin Type	Pin Numbers	Pull Up/Dn	Description
A0,1	I(TTL)	78,79/88,90	PU	A0,1 are the address inputs from the CPU. A0 generates SA0, while A1 and M/IO, S0, and S1 generate the CPU shutdown operation.
A17-23	I(TTL) O(B2)	104-110/116-122	PU	A17-23 are the input address lines from the CPU. These signals are used to decode the memory selection logic and can be output address lines of the memory mapper 74LS612.
AEN	O(B4)	139/157		DMA address enable signal. When High, AEN indicates that the DMA controller has control of the address, data, and read/write control buses.
BALE	O(B4)	85/97		Buffered Address Latch Enable signals the I/O slots that the present address is valid. SA0-19 is latched with the falling edge of BALE. BALE is forced High during DMA cycles.
BHE	I(TTL)	86/98	PU	Bus High Enable signal. BHE is active Low and is used to enable the High Byte of the data bus.
/BUSY	I(TTL)	122/138	PU	This input (active Low) should be connected to the BUSY output of the 80287.
/BUSY286	O(B2)	133/151		This is an active Low output that indicates the numeric processor 80287 is in operation mode. This pin is tied to busy input of the CPU.
CLK*2	I(TTL)	82/94	PU	This is the clock input and must be twice the desired processor clock frequency.
CNTLOFF	O(B2)	114/126		Control Off signal. When High, CNTLOFF enables the low byte data latch during 8-bit data transfer.
CPUHLDA	I(TTL)	119/132	PU	CPU Hold Acknowledge is the granting signal from the CPU to relinquish control of the system.
CPUHRQ	O(B2)	127/145		CPU Hold Request to the CPU for DMA and Refresh operation, active High.
/CS8042	O(B2)	138/156		Chip Select 8042 signal. When Low, /CS8042 selects the keyboard controller.
/DACK0-3 /DACK5-7	O(B2)	143-46/161-64 147-49/165-67		DMA Acknowledge signals. These signals are active Low and are used to acknowledge DMA requests (DRQ0-7)

Pin Symbols preceded by '/' are active low. Pin Type I = Input; O = Output; (TTL) = TTL level buffer; (CMOS) = CMOS level buffer. Pin Numbers to the left of '/' are for 160 pin flat pack. Numbers to the right are for the 180 pin PGA. PU = Pull Up; PD = Pull Down.

GC101 Peripheral Controller - Pin Description

Pin Symbol	Pin Type	Pin Numbers	Pull Up/Dn	Description
/DMAAEN	O(B2)	137/155		DMA Address Enable signal. /DMAAEN is active Low when a DMA access is in operation.
DRQ0-3 DRQ5-7	I(TTL)	150-53/168-71 154-56/172-74	PD	DMA Requests signals. These active High signals are used to request DMA services or control of the system. Each signal should be held High until the corresponding DACK signal goes Active. DRQ0-3 will perform 8-bit DMA transfer. DRQ4-7 will perform16-bit DMA transfer.
DT/R	O(B2)	115/127		Data Transmit/Receive signal. When High, DT/R indicates data flow from CPU to SD0-15 bus; when Low, DT/R indicates data flow in the opposite direction.
/ERROR	I(TTL)	121/136	PU	This signal is active Low when 80287 has an unmasked error condition.
HISPEED	I(TTL)	123/140	PU	When HISPEED is active (high), the processor clock will run at half the CLK*2 clock. Otherwise the processor clock will run at one fourth CLK*2. Bus I/O speed is handled separately.
INTR	O(B2)	130/148		INTerrupt Request from the master Interrupt Controller INT output, is active High.
/IOCHCK	I(TTL)	11/14	PU	I/O CHannel Check. This signal is active low and indicates an error condition from an I/O device. The error condition will interrupt the CPU when enabled through NMI (Non-Maskable Interrupt) output.
IOCRDY	I(TTL)	10/13	PD	I/O Channel Ready signal. IOCHRDY is held Low by the I/O or memory devices to lengthen the cycles by an integral number of clock cycles. This signal should not be held Low for more than 2.5 microseconds or memory data can be lost due to inadequate refresh.
/IOCS16	I(TTL)	13/16	PU	I/O Chip Select 16 signals the CPU that the data transfer is a 16-bit, one-wait state I/O cycle. This signal should be driven by open collector or 3-state driver.
/IOR	I(TTL) O(B4)	31/35	PU	I/O Read signal from 82288 to read from peripheral devices, active Low.
/IOW	I(TTL) O(B4)	32/36	PU	I/O Write signal from 82288 to write to peripheral devices, active Low. TTL Input Buffer.

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GC101 Peripheral Controller - Pin Description

Pin Symbol	Pin Type	Pin Numbers	Pull Up/Dn	Description
IOHALFSP	I(TTL)	124/142	PU	This signal controls the frequency of SYSCLK. When this signal is high and HISPEED is high, I/O will run at half the cpu clock. When HISPEED is low, I/O runs at the cpu clock speed. When IOHALFSP is low,I/O will run at the same speed as the cpu clock regardless of the state of HISPEED.
IRQ3-5 IRQ6-7 IRQ9-12 IRQ14-15	I(TTL) I(TTL) I(TTL) I(TTL)	157-159/176-178 1-2/2,4 4-7/7-10 8-9/11-12	PD	These are active High signals that interrupt the CPU.
/IRQ8	I(TTL)	3/6	PU	This signal is connected to the real time clock interrupt output.
/LSBEN	O(B2)	112/124		Least Significant Byte Enable signal. When Low, /LSBEN enables low-byte data.
/LCSROM	O(B4)	23/27		Latch Chip Select ROM signal, which selects the ROM address space 0E0000-0FFFFF and FE0000-FFFFFF.
/MASTER	I(TTL)	12/15	PU	/MASTER is an active Low signal and is used with the DRQ and DACK lines to gain control of the system. Upon receiving DACK, an I/O processor can pull /MASTER Low to gain control of the system address, data, and control buses.
M/IO	I(TTL)	87/99	PU	Memory I/O signal. When High, M/IO indicates a memory cycle; when Low, M/IO indicates an I/O cycle.
MBDIR	O(B2)	111/123		Memory Buffer Direction Signal. When MBDIR is High, data flows from MD0-15 to SD0-15; when MBDIR is Low, the data flows in the opposite direction.
/MDPCKN	I(TTL)	118/130	PU	Memory Data Parity Check signal. When Low, /MDPCKN indicates memory failure on parity test.
MDPCKE	O(B2)	117/129		Memory Data Parity Check Enable Signal. When High, MDPCKE selects parity checking logic.
/MEMCS16	I(TTL)	14/17	PU	Memory Chip Select 16 signals the CPU that the data transfer is a 16-bit, one-wait state I/O cycle. This signal should be driven by open collector or trisate driver.
/MEMR	I(TTL) O(B4)	28/32	PU	Memory Read signal. /MEMR is active Low during memory read and is 3-stated when CPUHLDA is High.

Pin Symbols preceded by '/' are active low. Pin Type I = Input; O = Output; (TTL) = TTL level buffer; (CMOS) = CMOS level buffer. Pin Numbers to the left of '/' are for 160 pin flat pack. Numbers to the right are for the 180 pin PGA. PU = Pull Up; PD = Pull Down.

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GC101 Peripheral Controller - Pin Description

Pin Symbol	Pin Type	Pin Numbers	Pull Up/Dn	Description
/MEMW	I(TTL) O(B4)	29/33	PU	Memory Write signal. /MEMW is active Low during memory write and is tristated when CPUHLDA is High.
/MSBEN	O(B2)	113/125		Most Significant Byte Enable signal. When Low, /MSBEN enables high-byte data.
NMI	O(B2)	129/147		Non-Maskable Interrupt signal. NMI is an active High signal that forces the CPU to execute the interrupt routine under any conditions.
/NPCS	O(B2)	131/149		Numeric Processor Chip Select signal. /NPCS is an active Low signal that ties to the NPS1 pin of 80287.
OSC	O(B4)	21/25		Oscillator is the 14.3818 MHZ color burst signal and is not synchronous with the SYSCLOCK.
OPTBUFUL	I(TTL)	125/143	PD	Output Buffer Full signal from keyboard controller P24. This signal is connected to IRQ1, which interrupts the CPU when the keyboard buffer is full.
/POWERG00D	I(CMOS)	25/29	PD	This signal, when Low, resets the controller. Schmitt Trigger Input.
PROCCLK	O(B8)	97/109		Processor Clock is the output signal that ties to the clock input of the CPU and the numeric processor.
RAM0RAS	O(B2)	33/37		This signal selects RAM bank 0 RAS control.
RAM1RAS	O(B2)	34/38		This signal selects RAM bank 1 RAS control.
RAM0CAS	O(B2)	35/39		This signal is the same as RAM0RAS except during refresh.
RAM1CAS	O(B2)	36/40		This signal is the same as RAM1RAS except during refresh.
RC	I(TTL)	126/144	PU	Reset CPU signal. This is an active Low signal from keyboard controller P21 and causes CPU shutdown.
/READY	O(B2)	128/146		/READY is an active Low signal that indicates to the CPU that the current bus cycle is near completion.
/REFRESH	I(TTL) O(B4)	17/20	NO	Refresh indicates the current cycle is for memory refresh and can be driven Low by devices on the I/O channel. Open Drain Outputs.

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G2

GC101/GC102

GC101 Peripheral Controller - Pin Description

Pin Symbol	Pin Type	Pin Numbers	Pull Up/Dn	Description
/RESET	O(B4)	22/26	NO	This signal is active Low and is used to reset system logic at power-up or low-line voltage outage. Open Drain Outputs.
RESETCPU	O(B2)	116/128		This is an active High signal that resets 80286 CPU during powerup, keyboard reset, and during a halt status.
RESET287	O(B2)	132/150		Reset 80287 is an active High signal that resets 80287 co-processor.
RSEL2	O(TTL)	76/84	PU	RAM Select 2 signal. When High, RSEL2 selects 1MBIT DRAM; when Low, RSEL2 selects 256K -bit RAM.
RSEL1,0	I(TTL)	75,74/83,82		RSEL 2,1,0 as follows: 0 0 0 selects 0-256K 0 0 1 selects 0-512K 0 1 0 selects 0-640K 0 1 1 selects 0-640K, 1M-1.384M 1 0 0 selects 0-512K 1 0 1 selects 0-640K 1 1 0 selects 0-640K, 1M-2.384M 1 1 1 selects 0-640K, 1M-4.384M
RTCAS	O(B2)	136/154		Real Time Clock Address Strobe signal. When Low, RTCAS latches the RAM address for Read/Write operations.
/RTCRD	O(B2)	134/152		Real Time Clock Read signal. When Low, /RTCRD data is read from the RTC
/RTCWR	O(B2)	135/153		Real Time Clock WRite signal. When Low,/RTCWR data is written to the RTC.
SA0	I(TTL)/O(B6)	30/34	PU	I/O Slot Address bus 0. This signal enables the low byte SD0-7.
SD0-15	I(TTL) O(B6)	37-54/41-62	PU	I/O Slot Data bus bits 0-15. These support 8/16 bit data transfer from I/O slots to CPU.
/SMEMR	O(B4)	26/30		System MEMory Read, which is the buffered version of /MEMR, active Low. 3-State Output Buffer
/SMEMW	O(B4)	27/31		System MEMory Write, which is the buffered version of /MEMW, active Low. 3-State Output Buffer
/S0,/S1	I(TTL)	83,84/95,96		Status 0,1 signals are used to convey the current CPU status to the 80288 bus controller

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G2

GC101/GC102

GC101 Peripheral Controller - Pin Description

Pin Symbol	Pin Type	Pin Numbers	Pull Up/Dn	Description
SPKR	O(B4)	24/28		Output of the Timer 8254 Channel 2.
SYSCLK	O(B4)	18/22		System Clock is synchronous with the CPU clock. See Table 1.
T/C	O(B2)	142/160		Terminal Count signal. T/C will pulse when the DMA channel terminal count is reached.
XA0	I(TTL) O(B4)	55/63	PU	External Address 0 is the signal that enables the Low byte of the data bus.
XA1-9 XA10-16	I(TTL)/O(B4) I(TTL)/O(B4)	56-66/64-74 67-73/75-81	PU	External Address 1-16 are the external address lines that tie to EPROM, keyboard, the numeric processor, etc. XA10-16 are 3-State Buffers.
XBHE	I(TTL) O(B4)	77/86	PU	External Bus High Enable signal activates the High byte of the data bus.
XD0-7	I(TTL) O(B4)	89-96/101-108	PU	External data bus bits 0-7. These support only 8-bit data transfers from external devices such as clock chip, serial port, etc., to CPU.
/XDEVEN	I(TTL)	81/93	PU	External Device Enable signal. /XDEVEN is an active Low signal that gates external devices to the SD bus.
/XMEMW /XMEMR /XIOW /XIOR	I/O(B4) I/O(B4) I/O(B4) I/O(B4)	99/111 98/110 103/115 102/114	PU	When /DMAAEN is not active, external memory and external I/O commands follow M/IO commands. When /DMAAEN is active, external M/IO commands have control of the operations. TTL Input Buffers
X1 X2	I(CMOS) I(B64)	16/19 15/18	NO	Xl and X2 are inputs tied to a 14.31818 MHz crystal to create OSC output.
0WS	I(TTL)	88/100		Zero Wait State is an active Low signal that cues the CPU to complete the present memory or I/O data transfer without inserting additional wait states. This signal should be driven by open collector or 3-state driver.

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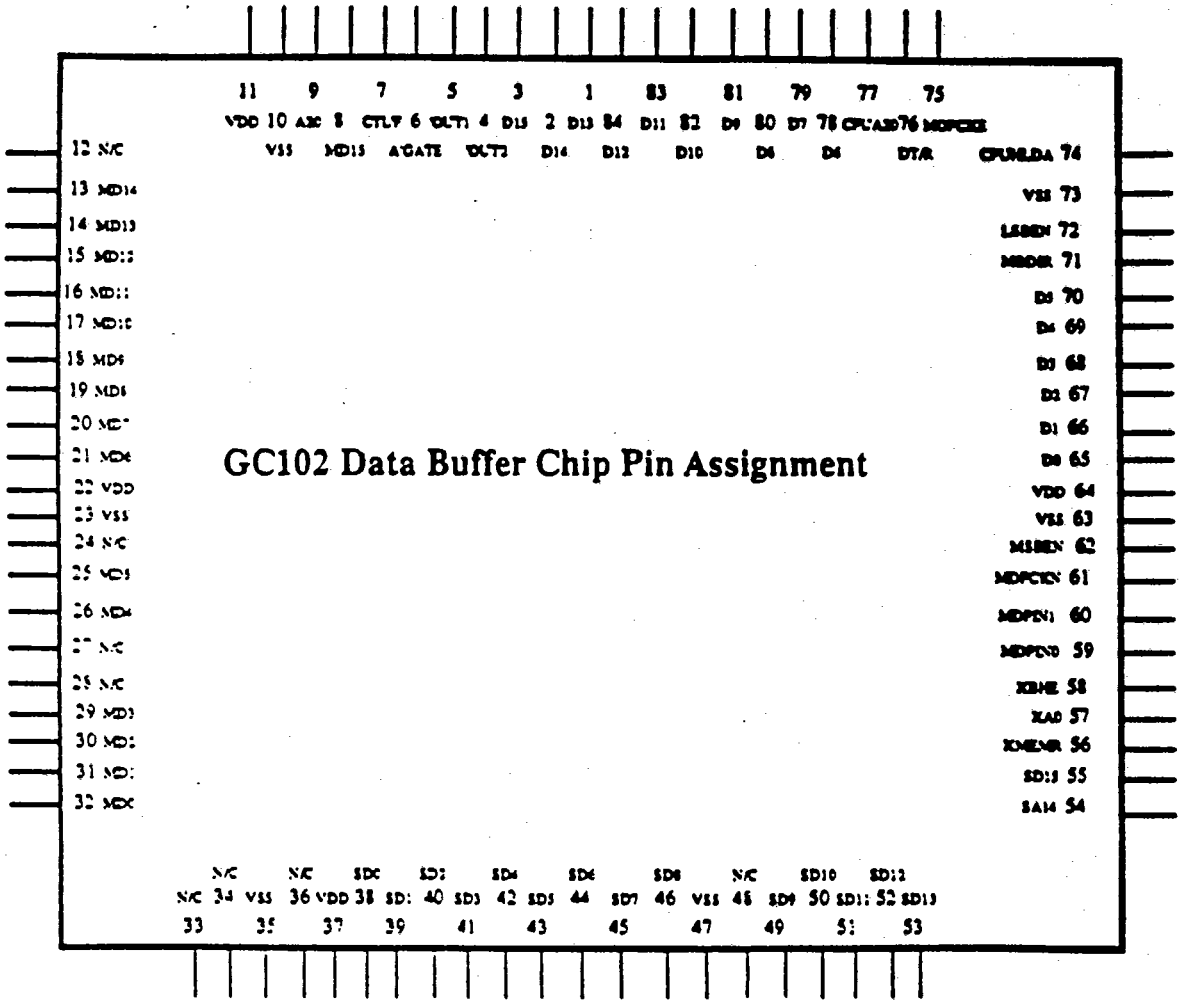
GC102 Data Buffer Chip

The GC102 Data Buffer chip buffers data for the CPU, the Expansion bus and the Memory data bus. Two signals control data flow direction. The DT/R signal controls data flow between the CPU data bus and the Expansion data bus. The MBDIR signal controls data flow between the Expansion bus and the Memory data bus.

Clocked by the CNTLOFF signal, latching is provided for data between the Expansion bus and the CPU bus.

The GC102 Data Buffer chip also includes parity logic circuitry. During memory read cycles, the parity bits for byte 0 and byte 1 from the RAMs are connected to pins MDPOUT0 and MDPOUT1 as the ninth input to the 9-bit parity error detect circuits. The other eight inputs come from the Memory data bus.

When the output signal MDPCKN is enabled and an error is detected on either byte 0 or byte 1 of the Memory data bus, MDPCKN will be active (low). During memory write cycles, parity bits for byte 0 and byte 1 are generated through on-board parity generator circuitry and then output through the MDPIN0 and MDPIN1 pins and written to RAM. (Pin 73 = VSS)



GC102 Data Buffer Chip Pin Assignment

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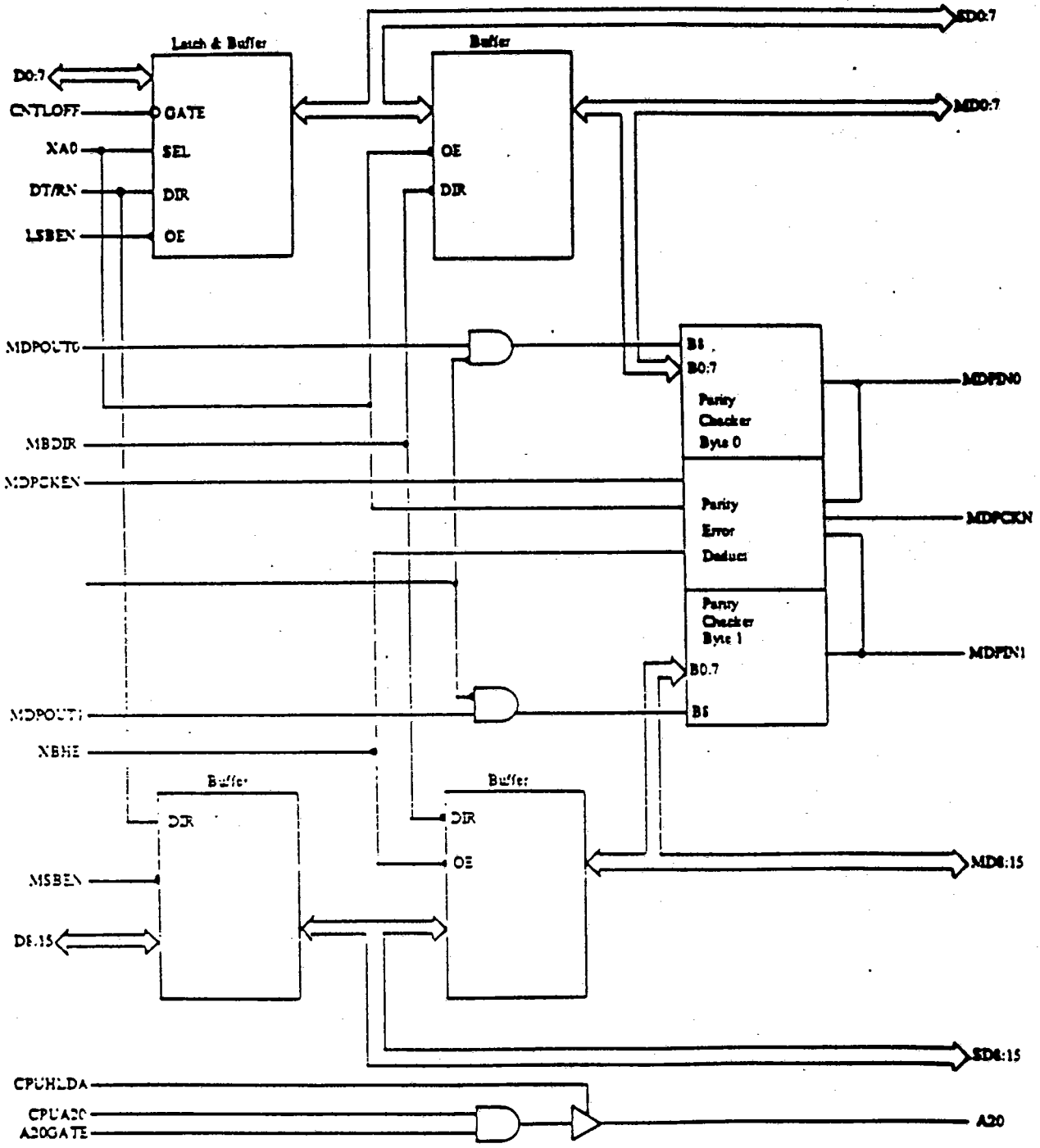
GC102 Data Buffer Chip Block Diagram



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GC102 Data Buffer - Pin Description

Pin Symbol	Pin Type	Pin Numbers	Pull Up/Dn	Description
A20	O(B12)	9		Address bit 20 of the CPU conditioned by A20GATE signal. 3-State Output Buffer.
A20G	I(TTL)	6		With a High on A20Gate and Low on CPUHLDA, A20 is the same state as that generated from the CPU. A Low on A20GATE and Low on CPUHLDA results in A20 being Low.
CNTLOFF	I(TTL)	7		An active High input to enable the low-byte data bus latch.
CPUA20	I(TTL)	77		Address bit 20 from CPU. This signal is conditioned by the A20GATE signal.
CPUHLDA	I(TTL)	74		CPU Hold Acknowledge signal. When High, the address bit 20 (A20GATE) is 3-stated. When CPUHLDA is Low, A20 is the same as the CPUA20 conditioned by A20GATE.
D0-D5 D6-D12 D13-D15	I/O(B6)	65-70 78-84 1-3	PU	Bidirectional Data Bus signals to and from the CPU.
DT/R	I(TTL)	76		Data Transmit/Receive signal. Indicates the direction of data flow between the D and SD buses. When DT/R is HIGH, data flows from D to SD. When DT/R is LOW data flows from SD to D.
/LSBEN	I(TTL)	72		Active Low to enable low-byte data transfer between D and SD buses.
MBDIR	I(TTL)	71		MD/SD bus directional control signal. When MBDIR is High, data flows from MD bus to SD bus; When MBDIR is Low, data flows from SD bus to MD bus.
MD0-MD3 MD4-MD5 MD6-MD14 MD15	I/O(B6) I/O(B6) I/O(B6) I/O(B6)	32-29 26-25 21-13 8	PU	On board memory data bus.
MDPCKE	I(TTL)	75		Memory Data Parity CheckK Enable signal. When High, MDPCKE enables the parity checking during memory read. TTL Input Buffer
/MDPCKN	O(B6)	61	PU	Memory Data Parity Check signal. Active Low to indicate a parity error during memory read.
MDPIN0 MDPIN1	O(B6)	59,60	PU	Memory data low and high parity bits. As generated, these signals are written into the RAMs during RAM write cycles.

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GC102 Data Buffer - Pin Description

Pin Symbol	Pin Type	Pin Numbers	Pull Up/Dn	Description
MDPOUT0 MDPOUT1	I(TTL)	4,5		Memory Data Low and High parity bit signals. These signals read data from the RAMs to generate parity check during read cycles.
/MSBEN	I(TTL)	62	PU	Active High to enable High-byte data transfer between D and SD buses. TTL Input Buffer.
VSS		10,23,35,47,63,73		GROUND
VDD		11. 22, 37, 64		POWER: +5 Volt Supply
[floating] [floating]		12. 24, 27-28 33-34, 36, 48		NOT CONNECTED NOT CONNECTED
SD0-SD8 SD9-SD15	I/O(B6)	38-46 49-55	PU	Expansion data bus, which makes possible data transfer between the D and MD buses.
XA0	I(TTL)	57		Local I/O bus address bit 0. This input enables the data transfer between the low byte of the SD and MD buses.
XBHE	I(TTL)	58		Local I/O Bus High Enable signal. This signal enables the data transfer between the high byte of the SD and MD buses.
/XMEMR	I(TTL)	56		Memory Read signal. This input enables the parity circuit during RAM read operations.

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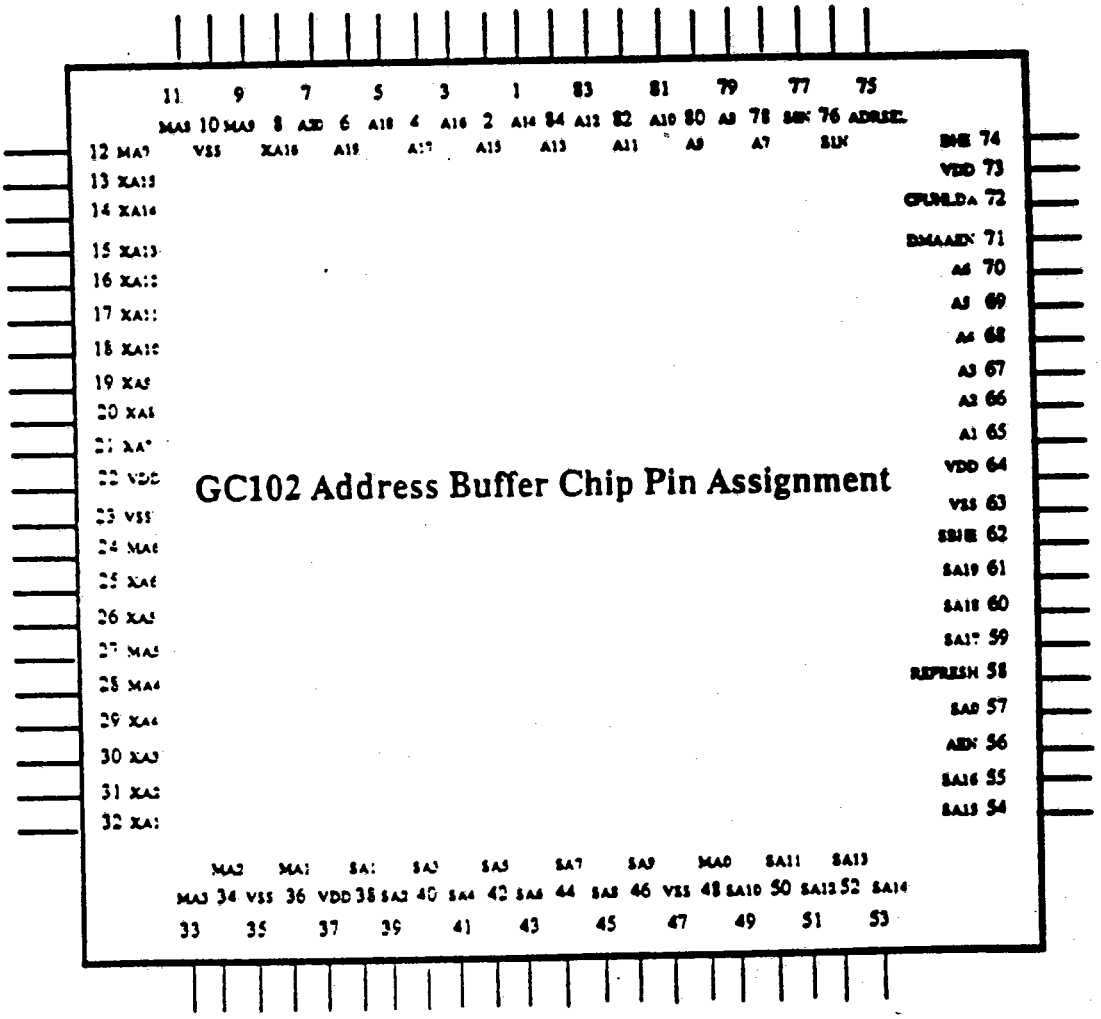
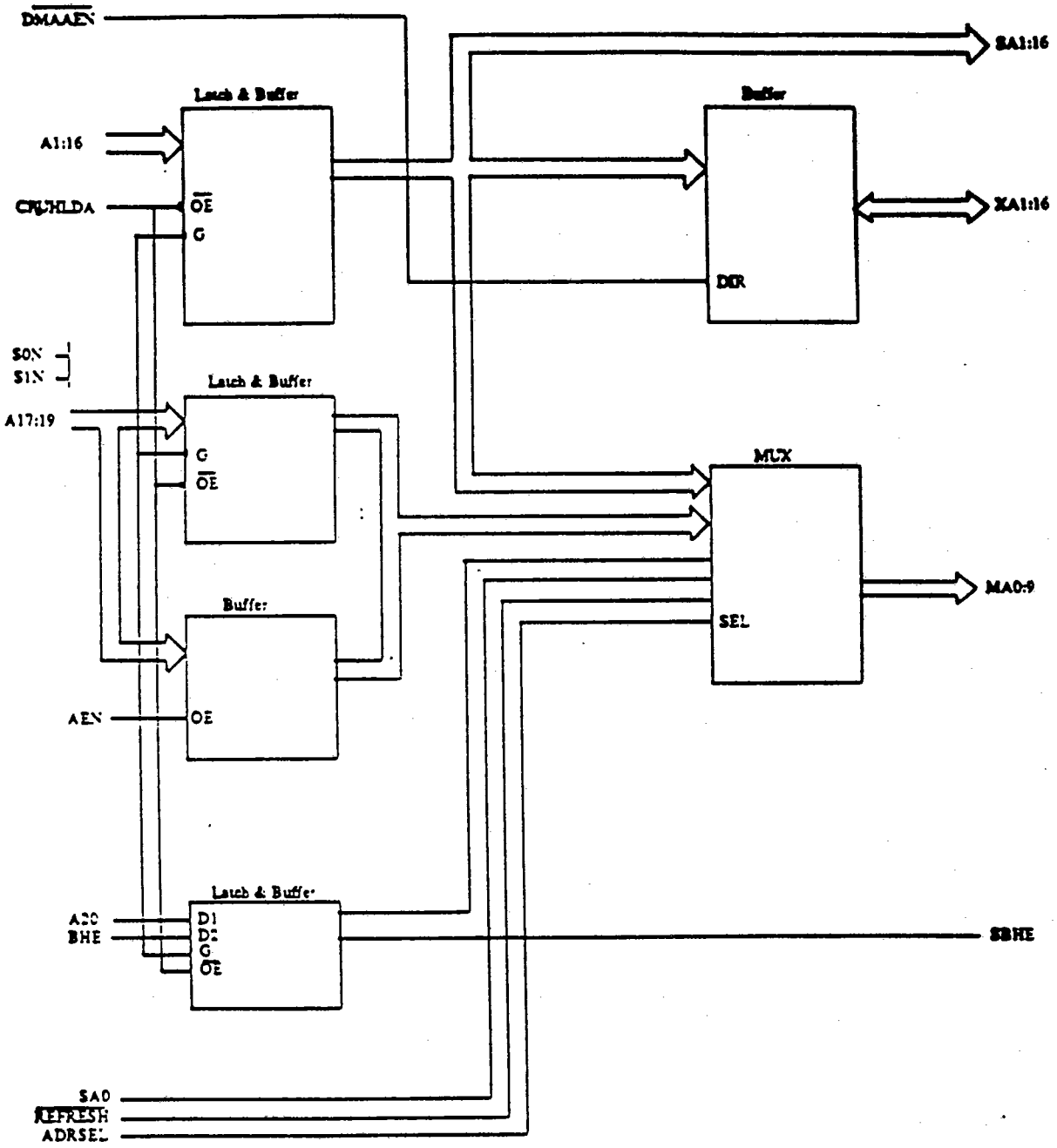
GC102 Address Buffer Chip

The GC102 Address Buffer chip provides address buffers for the Expansion bus, the Local I/O bus and the system board DRAMs. Early ALE is included to latch the address from the CPU. The /DMAAEN signal controls the address flow direction between the Expansion bus and Local I/O bus. The CPUHLDA signal controls the direction of address flow from the CPU to the Expansion bus. By multiplexing the address bits of the Expansion bus (via ADRSEL and /REFRESH), the Memory address bus (MA0:9), which drives the system board DRAMS, is generated. Ten bits of address allow for either 256K or 1 Mbit DRAMs. (Pin 73 = VDD)



GC102 Address Buffer Chip Pin Assignment

GC102 Address Buffer Chip Block Diagram



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GC101/GC102

GC102 Address Buffer - Pin Description

Pin Symbol	Pin Type	Pin Numbers	Pull Up/Dn	Description
A1-A6	I(TTL)	65-70	PU	Address input signals from CPU. These are latched when both /S0 and /S1 are High.
A7-A13	I(TTL)	78-84		
A14-A16	I(TTL)	1-3		
A17-A20	I(TTL)	4-7		
ADRSEL	I(TTL)	75		Address Select signal. ADRSEL controls the generation of the RAS and CAS addrresses on the MA bus for addressing the system RAMs.
AEN	I(B6)	56	PU	Address Enable signal. This pin conveys the A17-A19 signals directly into SA17-SA19, respectively.
BHE	I(TTL)	74		Bus High Enable signal. Transmitted from the CPU, BHE indicates a data transfer on the most significant byte of the bus.
CPUHLDA	I(TTL)	72		CPU Hold Acknowledge signal. When CPUHLDA is Low, the address latches drive the SA bus.
DMAAEN	I(TTL)	71		DMA Address ENable signal. DMAAEN controls the direction of data transfer between SA and XA buses. When DMAAEN is High, data flows from SA to XA.
MA0	O(B12)	48		Address signals for addressing system RAMs;
MA1	O(B12)	36		MA9 is for 1MB DRAMs.
MA3-MA2	O(B12)	33,34		3-State Output Buffers
MA5-MA4	O(B12)	27,28		
MA6	O(B12)	24		
MA8-MA7	O(B12)	11,12		
MA9	O(B12)	9		
/REFRESH	I(TTL)	58		Refresh active LOW signal. This signal selects SA0 as MA6 during refresh.
SA0	I(TTL)	57		Address bit 0 signal. SA0 is used during refresh. Bidirectional signals
SA1-SA9	I/O(B6)	38-46		for the expansion bus.
SA10-SA16	I/O(B6)	49-55		
SA17-SA19	I/O(B6)	59-61		
SBHE	O(B6)	62	PU	Bus High Enable signal for the expansion bus. This signal is the output of the BHE latch.
/S1	I(TTL)	76		CPU Status output signals. /S1 and /S0 generate the clock signals for
/S0	I(TTL)	77		the address latches in this chip.
VSS		10, 23, 35, 47, 63		GROUND

Pin Symbols preceded by '/' are active low. Pin Type I = Input, O = Output; (TTL) = TTL level buffer; (CMOS) = CMOS level buffer. PU = Pull Up PD = Pull Down.

G2

GC101/GC102

GC102 Address Buffer - Pin Description

Pin Symbol	Pin Type	Pin Numbers	Pull Up/Dn	Description
VDD		22, 37, 64, 73		POWER: +5 Volts Supply
XA1-XA4	I/O(B6)	32-29	PU	Peripheral address signals for the local bus
XA5-XA6	I/O(B6)	26-25		
XA7-XA15	I/O(B6)	21-13		
XA16	I/O(B6)	8		

Pin Symbols preceded by '/' are active low. Pin Type I = Input; O = Output; (TTL) = TTL level buffer; (CMOS) = CMOS level buffer. PU = Pull Up. PD = Pull Down

GC102 Address Buffer Chip -- AC Characteristics

Input	Output	Typical (ns)	WCCOM (ns)
any A	any SA	9.95	18.6
BHE	SBHE	8.76	16.4
S0 or S1	any SA	11.77	22.0
CPUHLDA	any SA	10.58	21.2
CPUHLDA	SBHE	8.46	15.8
AEN	SA17,18,19	10.78	20.2
any SA	any XA	8.49	15.9
any XA	any SA	8.39	15.7
any SA (SA0)	any MA MA8	7.45 8.38	14.0 15.7

Input	Output	Typical (ns)	WCCOM (ns)
any XA	any MA	8.64	16.2
DMAAEN	any XA	11.92	22.3
DMAAEN	any SA	10.69	20.0
REFRESH	MA	8.05	15.1
ADRSEL	MA MA8	8.29 9.40	15.5 17.6
any A	MA MA8	10.22 11.50	19.1 21.5

GC 101 / GC102 Chip Set - DC Characteristics

Specified at VDD = 5V +/-5% over the commercial temperature range (0-70C).

Symbol	Parameter	Condition	Min	Max	Units
VIL	Voltage Input LOW - TTL Inputs			0.8	V
VIH	Voltage Input HIGH -TTL Inputs		2.0		V
IIN	Input Current, TTL, CMOS Inputs	Vin = Vdd or Vss	-10	10	uA
	Inputs with Pull Down Resistors	Vin = Vdd	10	120	uA
	Inputs with Pull Up Resistors	Vin = Vss	-100	-8	uA
IDD	Quiescent Supply Current	Vin = Vdd or Vss		4	mA

G2 Application Note

GC101/102 Configuration Options

AT compatible systems implemented using the G2 AT chipset (Models GC101 and GC102) offer several different configuration options. Those options involve the processor clock speed, options to slow down the expansion bus to insure expansion board compatibility, and options for suppor of 256k or 1Mbit DRAMS. This paper elaborates on those options

HISPEED

This option allows the user to change the CPU speed dynamically either from a switch mounted on the front panel or if supported by the keyboard controller firmware, through the system keyboard. In a 16 MHz system, the oscillator for the CPU will normally be 32 MHz. The output of the oscillator is buffered by the peripheral controller and then feed to the CLK input of the 80286 CPU. When the HISPEED input of the controller chip is low, the 32 MHz clock is divided by two before feeding to the CLK input of the CPU. Internal circuitry will ensure the synchronization of the change-over of frequency to the CPU and will not affect the operation of the software that is running on the system.

IOHALFSP

This signal allows the use of lower speed peripheral cards to be used in the higher speed G2 system. When this option is selected (IOHALHSP = 1 and HISPEED = 1), The signal SYSCLK at the expansion bus will change frequency depending on the instruction being executed by the CPU. In a 16 MHz system, the SYSCLK signal will normally run at 16 MHz, when the controller detects that an I/O instruction is being executed, the SYSCLK frequency will be divided by two. The peripheral card will operate as if the system is running at half the CPU speed or 8 MHz. Note that the slow down of the SYSCLK only occurs at I/O instructions. SYSCLK will continue to run at full speed during instruction fetch, memory read write and CPU internal operation as long as it is accessing the on board RAM as set by DIP switches SEL0,SEL1 and SEL2. For a 12 MHz system, the I/O half speed option will force I/O operation to the expansion slots to an equavalent speed of 6 MHz during the reading or writing to IO ports on these expansion boards. The video memory or system memory on these boards can operate at one wait state if the MEMCS16 signal at the expansion is slot is pulled low. Or, if the 0WS signal is pulled low, expansion memory can operate at zero wait states.

In the case of a line printer operating at 200 CPS with a parallel interface, five milli seconds are available for the system to test if the printer is ready for another character and to send the character. This is sufficient time for the system to respond. In the case of other peripherals there are usually only a few registers that are accessed using I/O instructions and they usually written to only one time. The lowering of the SYSCLK to half of the CPU speed will allows slower devices to be used on the system and have only a very minor impact on system throughput. Also note that IOHALFSP input is only valid when HISPEED is at a 1. When HISPEED is at logic 0, the system is running at half speed and IOHALHSP input will have no effect on the system.

RSEL2

This input selects the type of DRAM to be used in the system. When RSEL2 is high, 1M-bit DRAMs can be used on the system. When RSEL2 is low, 256K-bit DRAM must be used.

RSEL1,0

These two signals control the address mapping on the system board. For systems using 256K DRAM, the mapping is as follows:

RSEL	1	0	
	0	0	0-256K
	0	1	0-512K
	1	0	0-640K
	1	1	0-640K, 1M - 1.384M

For system with 1M-byte of memory, connecting RSEL 0 and 1 to logic high will map the first 640K of memory to address 0 to 640K of the system. The remaining 384K will be mapped to the memory space 1M to 1.384M. This frees up the memory location from 640K to 1M for system use.

For system using 1 M-bit DRAM:

RSEL	1	0	
	0	0	0-512K
	0	1	0-640K
	1	0	0-640K, 1M - 2.384M
	1	1	0-640K, 1M - 4.384M

Application Note

Memory Expansion / IRQ Lines / Delay Line

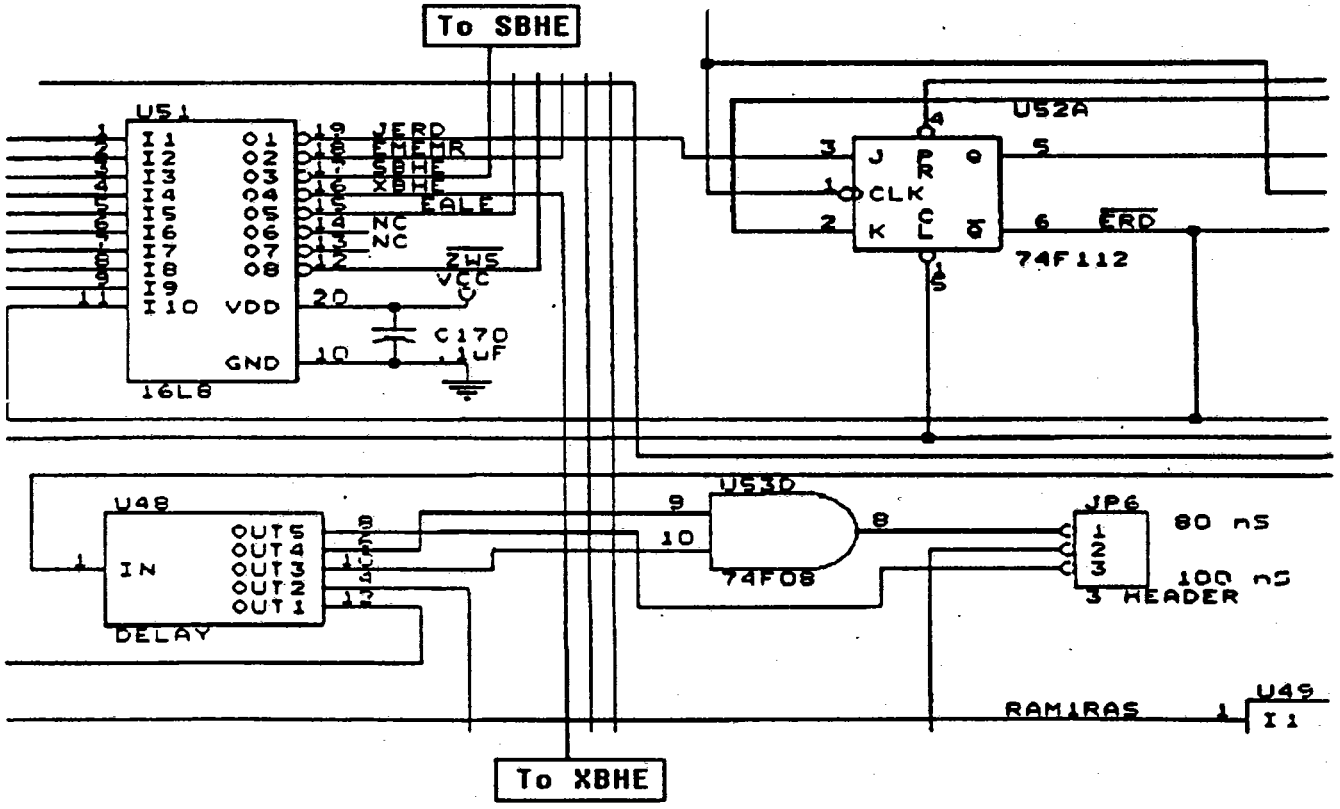
AT compatible system boards designed with the GC101/102 according to schematics published prior to March 16, 1988 will require require several modifications to ensure the highest degree of compatibility with OS/2, common expansion boards, and delay lines used in manufacturing.

Running OS/2 on the G2 System Board

In order to guarantee compatibility with IBM OS/2 on boards designed prior to mid March 1988, it will be necessary to make a minor change to one of the PAL equations (U51) and add two jumpers: U51 pin 17 to JC pin 1 (SBHE), and U51 pin 16 to U49 pin 11 (XBHE). The diagram below shows these modifications to sheet 9 of the 286 motherboard schematic dated before March 16 1988. .

Modification to Delay Line Circuit

In order to render superior tolerance to the wide range of delay line specifications available from leading suppliers, it is necessary to add a single gate to the circuit between the delay line (U48) and JP6. This change is also reflected in the diagram below.



IRQ Pullup Resistors.

All evaluation board implementations of G2's GC101/102 designed by G2 prior to March 1988 lacked pullup resistors on all I/O channel IRQ lines (specifically IRQ3,4,5,6,7,9,10,11,12,14 and 15). A pullup resistor to +5V with a value of 10k ohms should be added to each of these lines. This was the cause of several minor incompatibility problems with some expansion boards.

G2

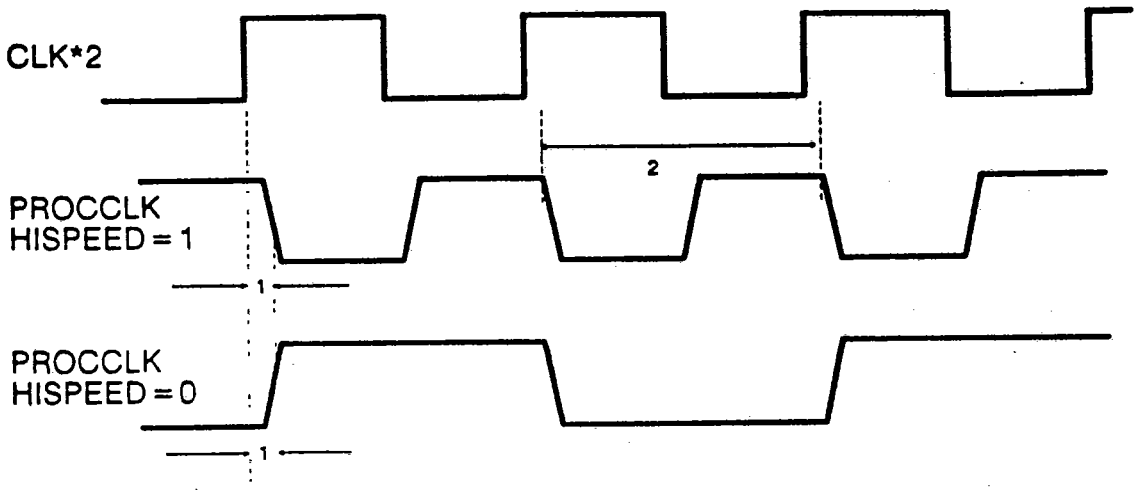
GC101/GC102
Timing Diagrams

Key to Timing Diagrams

GC101 TIMING			TEST
	MIN	MAX	COND
1 PROCCLK DELAY		21ns	85pf
2 PROCCLK PERIOD	31ns		85pf
3 SYSCLK		10ns	85pf
4 S0,S1 SETUP TIME	13ns		85pf
5 S0,S1 HOLD TIME	0ns		85pf
6 BALE DELAY	9ns		50pf
7 /MEMR DELAY		10ns	85pf
8 /MEMW DELAY		10ns	85pf
9 DT/R DELAY		9ns	25pf
10 /IOR DELAY		17ns	85pf
11 /IOW DELAY		17ns	85pf
12 /MEMCS16 SETUP TIME	6ns		85pf
13 /MEMCS16 HOLD TIME	0ns		85pf
14 /M/IO SETUP TIME	16ns		85pf
15 /M/IO HOLD TIME	0ns		85pf
16 BHE SETUP TIME	2ns		85pf
17 /IOCS16 SETUP TIME	9ns		85pf
18 /IOCS16 HOLD TIME	0ns		85pf
19 RAM0RAS, RAM1RAS DELAY		14ns	25pf
20 RAM0CAS, RAM1CAS DELAY		14ns	25pf
21 0WS SETUP TIME	12ns		85pf
22 0WS HOLD TIME	0ns		85pf
GC102 TIMING	16MHz/1ws	12MHz	
	12MHz/0ws	1ws	
23 MA BUS TO ALE DELAY	12ns	24ns	85pf
24 MD TO D BUS DELAY	12ns	16.5ns	85pf

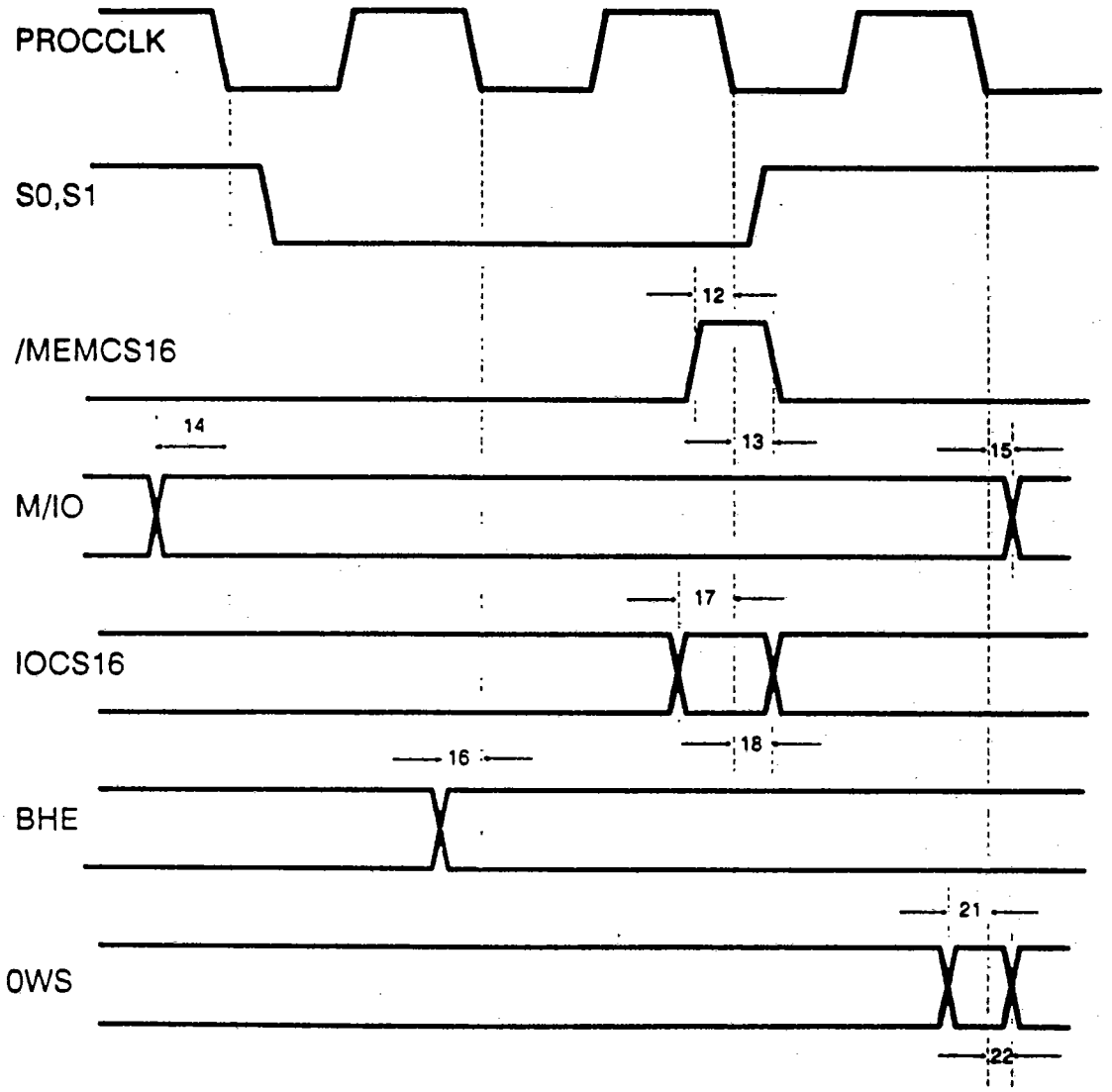
GC101/GC102
Timing Diagrams

GC101 Clock Timing



GC101/GC102
Timing Diagrams

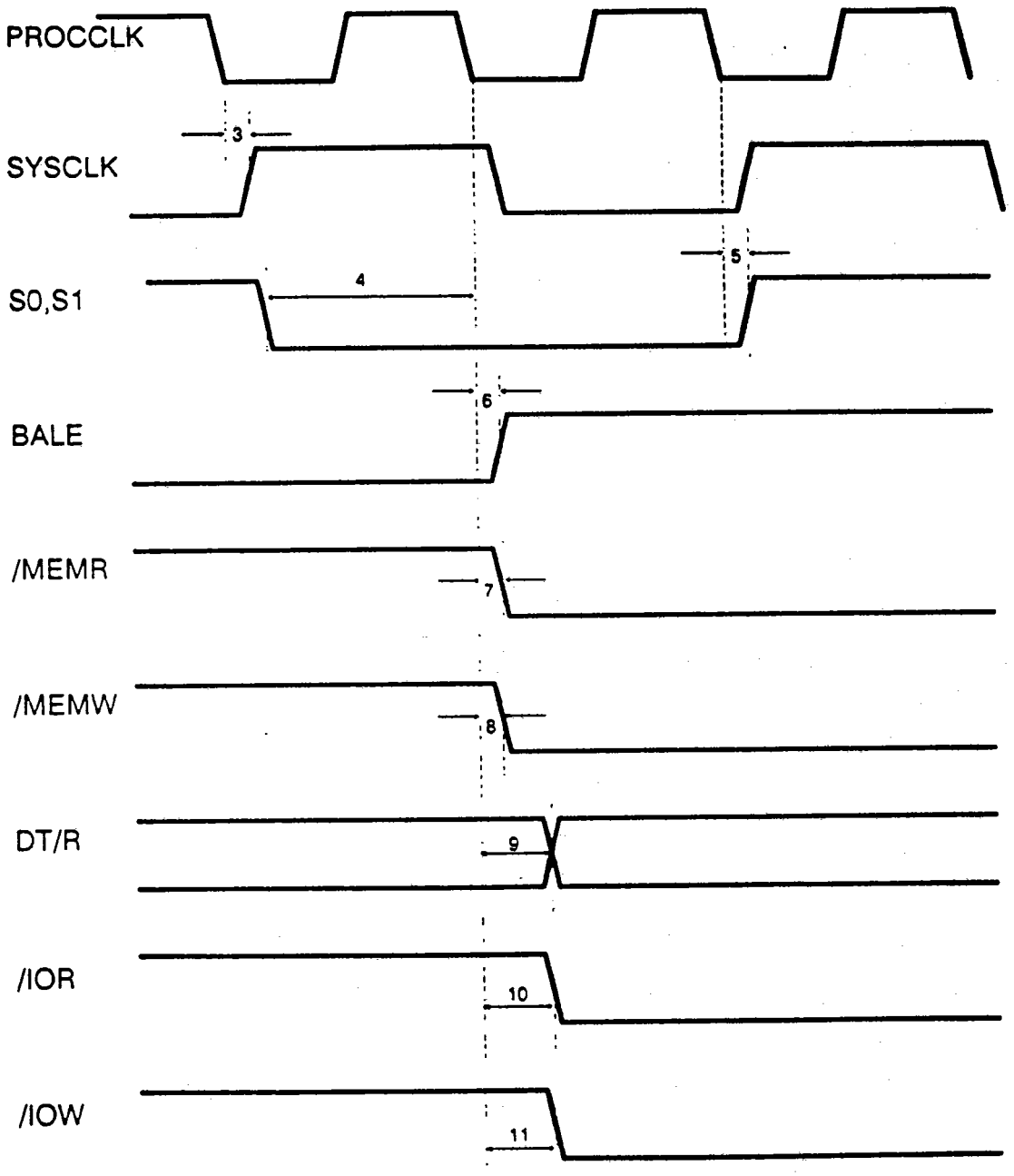
GC101 Input Signal Timing



G2

GC101/GC102
Timing Diagrams

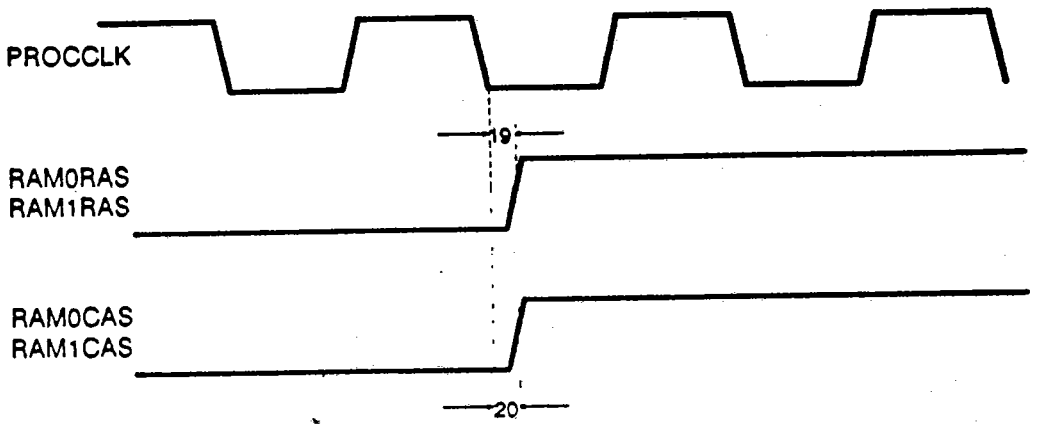
GC101 Control Signal Timing



G2

GC101/GC102
Timing Diagrams

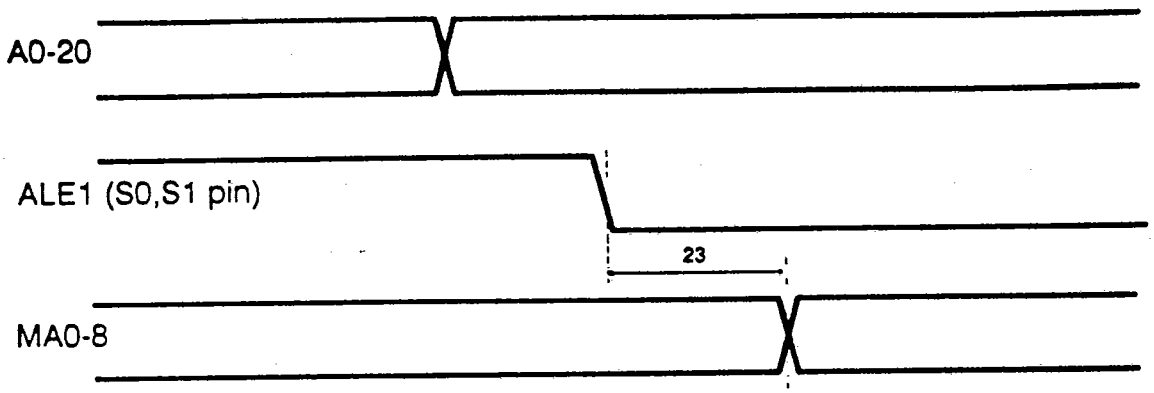
GC101 Output Signals



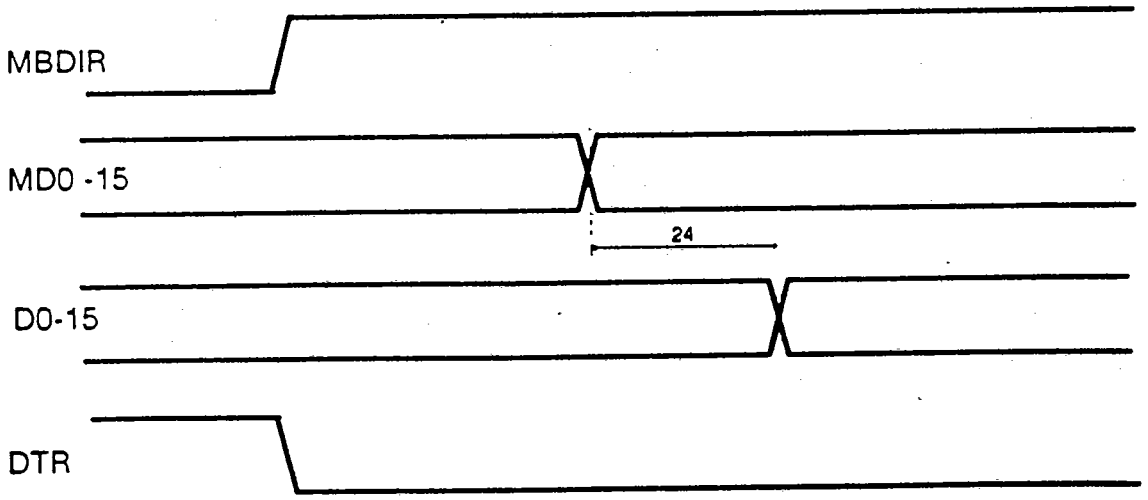
G2

GC101/GC102 Timing Diagrams

GC102 Address Buffer



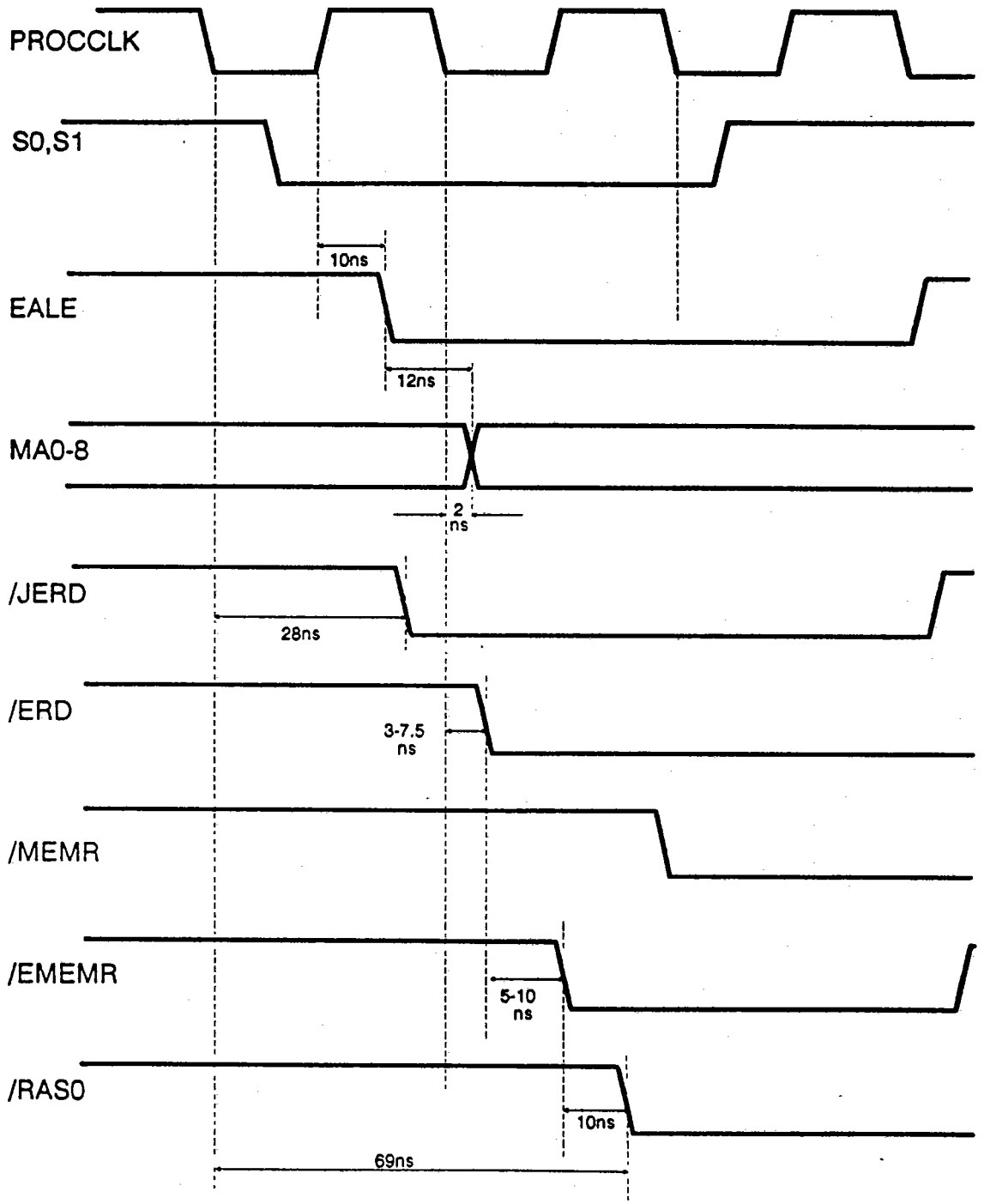
GC102 Data Buffer



G2

GC101/GC102
Timing Diagrams

GC101 12MHz Zero Wait State Timing



GC101/GC102
Device List for Production Board

3777475 G-TWO (2) INC 02E 00093 D T-49-17-01

ITEM	QTY	PART-NAME	REFERENCE-DESIGNATOR	DESCRIPTION
1	1	GC102DAT	U33	
3	1	HC39	Y3	VAL=32.768KHz
5	5	R40	R18 R30 R28 R22 R24	VAL=1K
6	10	R40	R20 R21 R19 R5 R6 R26 R32 R23 R2 R33	VAL=10K
7	2	R40	R11 R16	VAL=30
8	1	R40	R27	
9	4	R40	R15 R14 R29 R13	VAL=300
10	1	R40	R9	VAL=2M
11	1	R40	R8	VAL=100
12	2	R40	R10 R7	VAL=15
13	2	R40	R12 R17	VAL=2.0M
14	2	R40	R3 R4	VAL=150
15	1	R40	R1	VAL=330
16	1	R40	R25	VAL=51K
17	1	R40	R31	VAL=470
19	1	RSIP10BA	Z4	VAL=30
21	1	DIPSW4	S1	
23	1	GC102ADD	U46	
25	1	80287	U51	
27	1	BATTH2	B1	
29	2	1N60	CR1 CR4	
31	2	27256	U44 U45	
33	1	74F08	U32	

GC101/GC102
Device List for Production Board

3777475 G-TWO (2) INC 02E 00094 D T-49-17-01

ITEM	QTY	PART-NAME	REFERENCE-DESIGNATOR	DESCRIPTION
35	1	COR020	C41	VAL=100pF
36	1	COR020	C42	VAL=50pF
37	1	COR020	C94	VAL=27pF
38	2	COR020	C59 C60	VAL=15pF
39	1	COR020	C77	VAL=4.7nF
41	1	HC18	Y1	VAL=14.318MHz
42	1	HC18	Y2	VAL=8.000MHz
44	5	1X3PIN	W6 W1 W3 W2 W4	
46	1	GC101160	U47	
48	6	CON36EMB	J2CD J3CD J4CD J6CD J7CD J1CD	
50	8	CON62EMB	J3AB J4AB J5AB J6AB J7AB J8AB J2AB J1AB	
52	1	74ALS245	U50	
54	2	2N3904	Q1 Q3	
56	23	CER010	C96 C100 C97 C3 C99 C98 C61 C72 C92 C86 C84 C66 C82 C80 C1 C15 C38 C70 C90 C88 C68 C64 C134	VAL=10uF
58	1	MC146818	U52	
60	1	MC14069	U53	
62	1	RSIP8AA	Z5	VAL=10k
64	1	2N3906	Q2	
66	2	RSIP8BA	Z2 Z1	
67	1	RSIP8BA	Z3	VAL=30
69	2	MOLEX6	P5 P6	

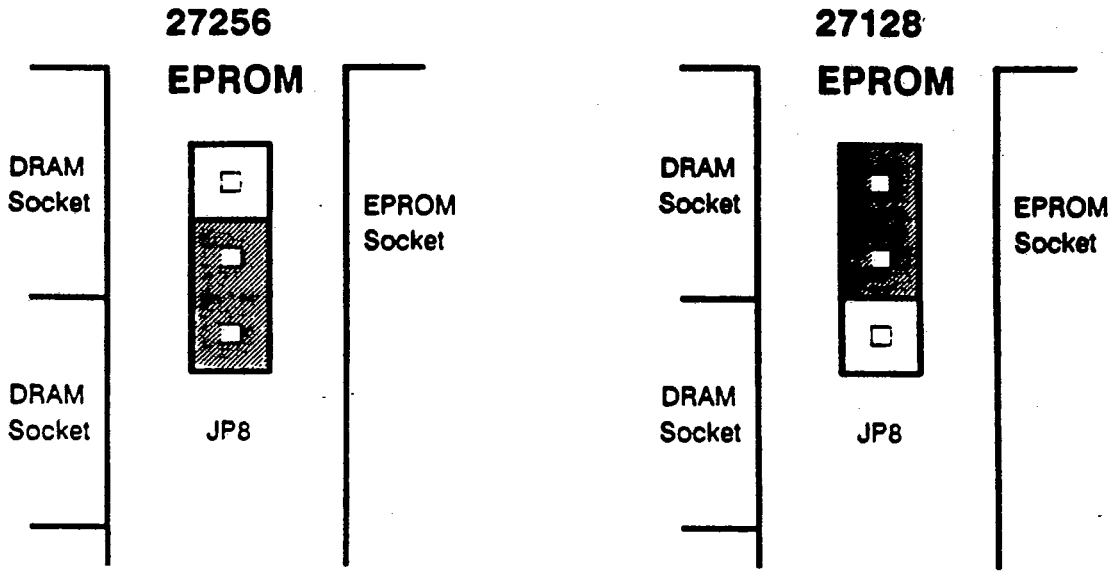
GC101/GC102
Device List for Production Board

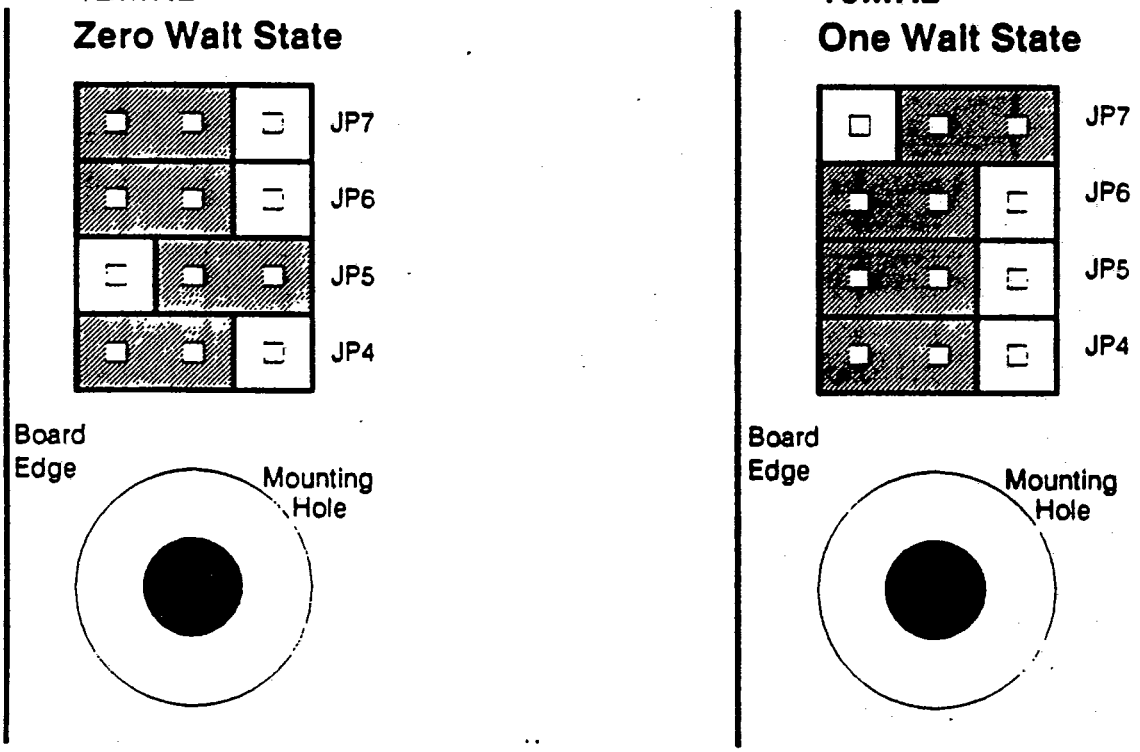
ITEM	QTY	PART-NAME	REFERENCE-DESIGNATOR	DESCRIPTION
71	1	1N4148	CR5	
73	2	1N914	CR3 CR2	
75	1	DELAY4	U20	
77	1	80286	U49	
79	36	4125610	U14 U10 U5 U1 U15 U11 U6 U2 U16 U12 U7 U3 U17 U13 U8 U4 U9 U18 U38 U34 U25 U21 U39 U35 U26 U22 U40 U36 U27 U23 U41 U37 U28 U24 U29 U42	
81	1	8742	U48	
83	1	7406	U54	
85	2	1X4PIN	P7 P1	
87	2	L040	L1 L2	VAL=2.2uH
89	1	TXCO	UA3	VAL=25.000MHz
91	4	1X2PIN	W7 P4 W5 P2	
93	2	16L8	U31 U30	
95	1	74F112	U19	
97	1	1X5PIN	P3	
99	2	RSIP6AA	Z6 Z7	VAL=10K
101	1	COA030	C2	VAL=.01uF
102	98	COA030	C78 C17 C8 C4 C22 C18 C9 C5 C23 C19 C10 C6 C24 C20 C11 C12 C25 C21 C44 C33 C29 C49 C45 C34 C30 C50 C46 C35 C31 C51 C47 C36 C32 C37 C52 C48 C28 C62 C63 C26 C27 C13 C14	VAL=.1uF

GC101/GC102
Device List for Production Board

ITEM	QTY	PART-NAME	REFERENCE-DESIGNATOR	DESCRIPTION
			C39 C53 C16 C40 C130 C126 C122 C118 C114 C110 C106 C103 C129 C125 C121 C113 C109 C105 C102 C131 C128 C127 C124 C120 C112 C108 C104 C101 C123 C119 C115 C111 C107 C87 C71 C89 C73 C91 C93 C65 C81 C67 C83 C69 C85 C79 C7 C54 C56 C74 C55 C75 C58 C43 C57	
103	2	COA030	C132 C133	VAL=47pF
104	3	COA030	C95 C117 C116	
105	1	COA030	C76	VAL=.047uF
107	1	5PDINF	J9	

GC101/GC102
Jumper Settings for Production Board





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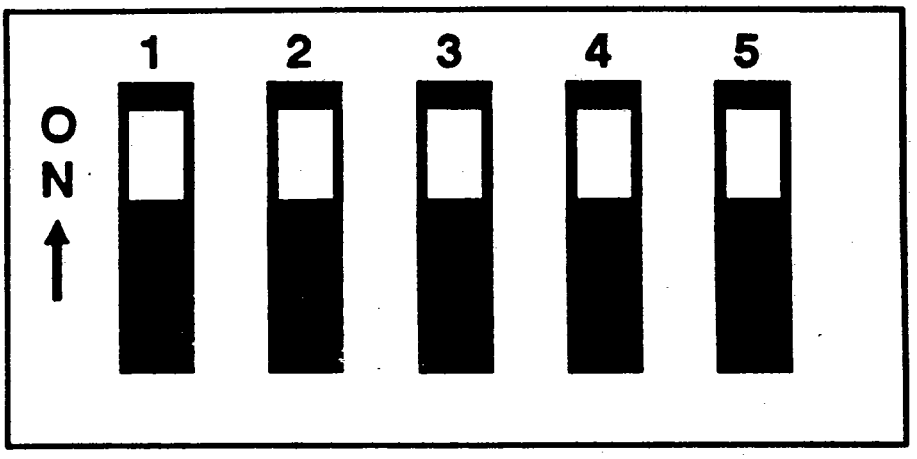
GC101/GC102
Switch Settings for Production Board



SW1

1 - HISPEED

2 - I/O HALF SPEED

3 - RSEL0

4 - RSEL1

5 - RSEL2

Jumper functions and setting for 286 system board

J1 EXTERNAL BATTERY CONNECTOR
1 = POSITIVE
2 = NC OR KEY
3 = GROUND
4 = GROUND

J2 LOUD SPEAKER CONNECTION
1 = OUTPUT
2 = NC OR KEY
3 = GROUND
4 = + 5V

J3 KEYBOARD

J4 MISC
1 = LED POWER
2 = NC OR KEY
3 = GROUND
4 = KEYBOARD INHIBIT
5 = GROUND

JP1 RESET

JP2 HI-SPEED OR TURBO LED

JP3 MONOCHROME / COLOR

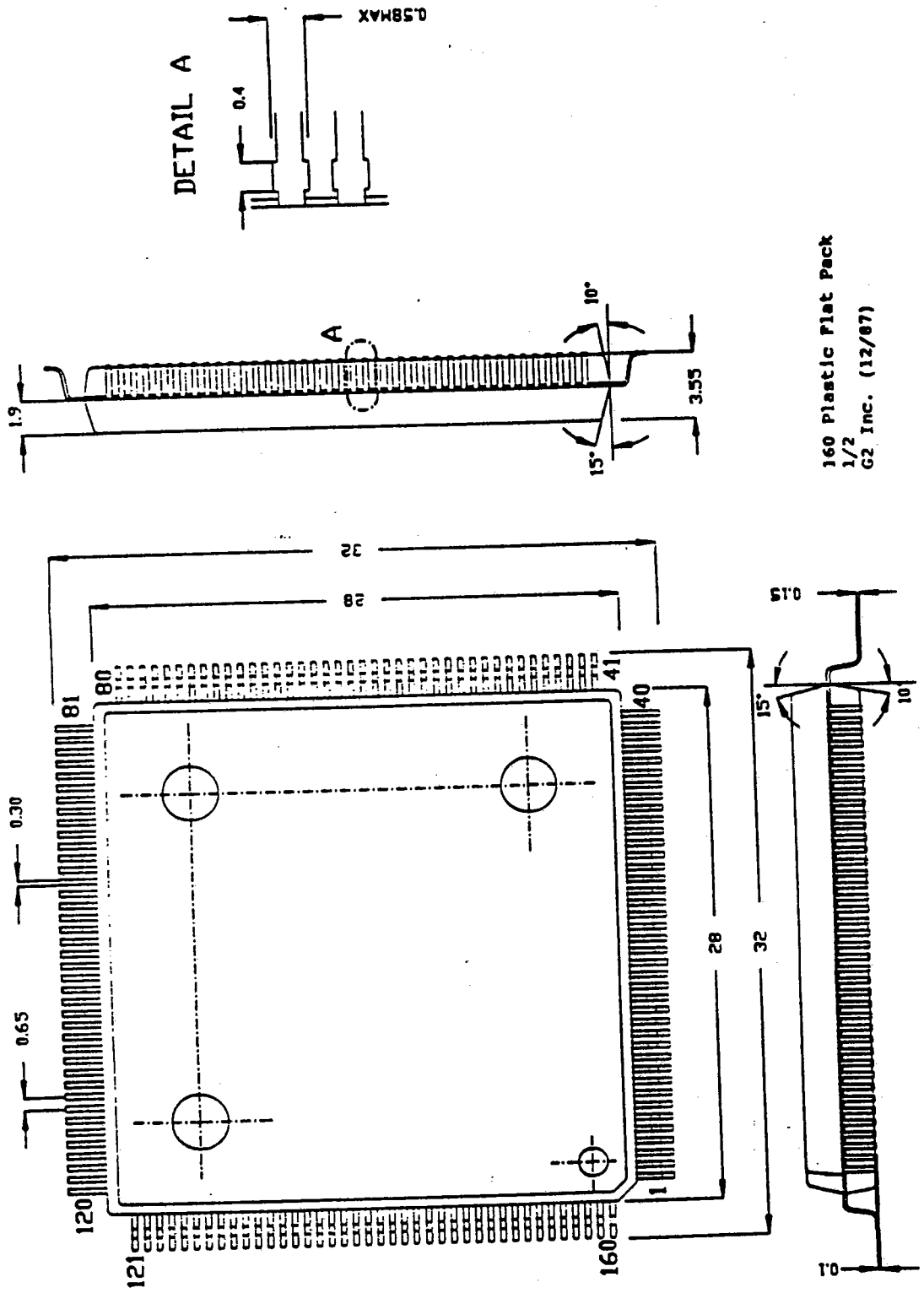
JP4 EMEMW SELECT - SELECT 2 AND 3 ALWAYS

JP5 CLOCK DELAY SELECTION
1-2 FOR 16 MHZ
2-3 FOR 12 MHZ

JP6 DELAY LINE JUMPER - SELECT 1 AND 2 ALWAYS

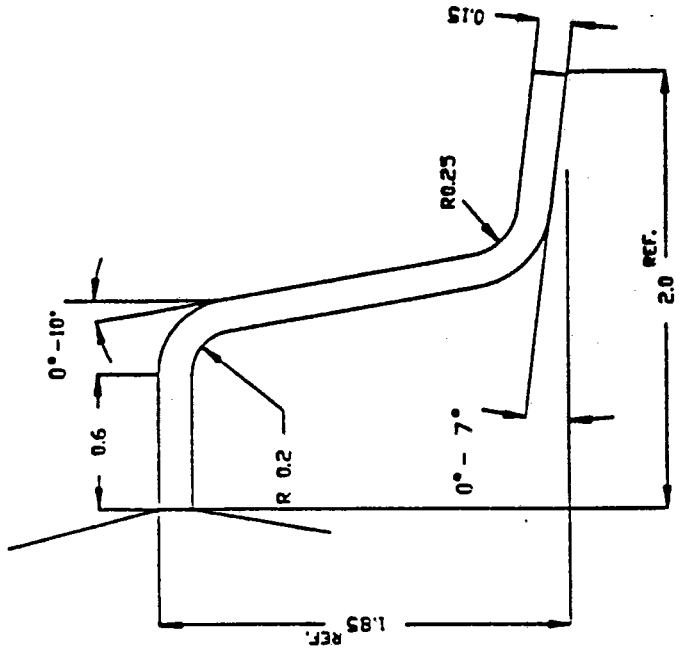
JP7 ZERO WAIT STATE SELECTION
1-2 FOR 0WS
2-3 FOR 1WS

GC101/GC102
Package Outlines

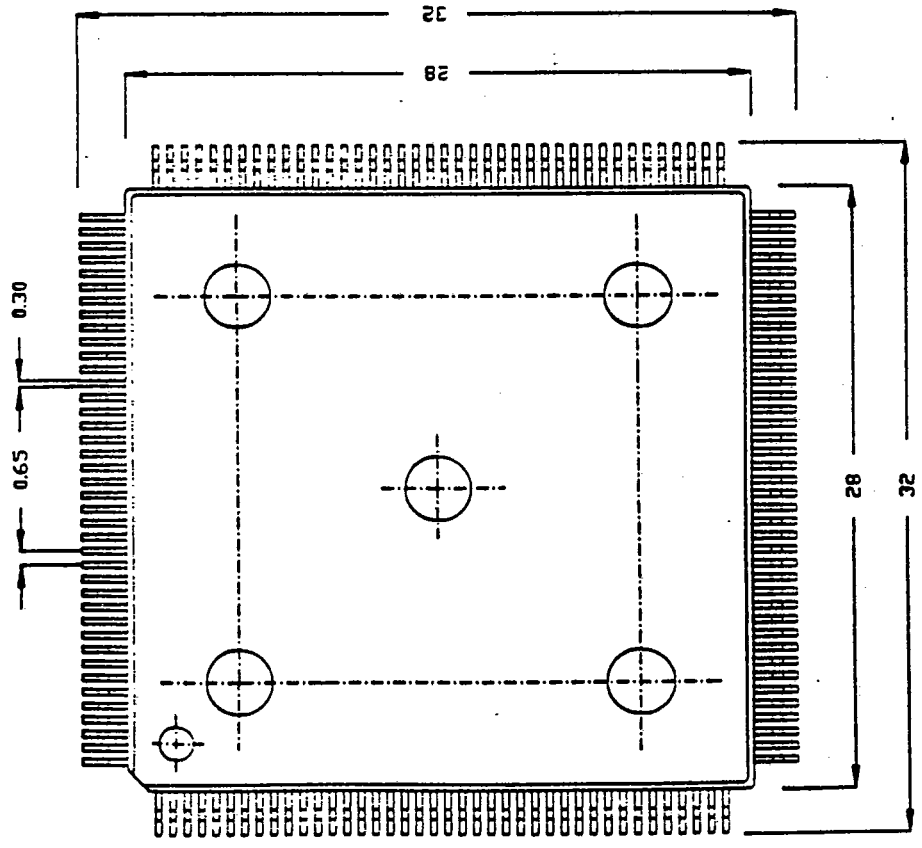


G2

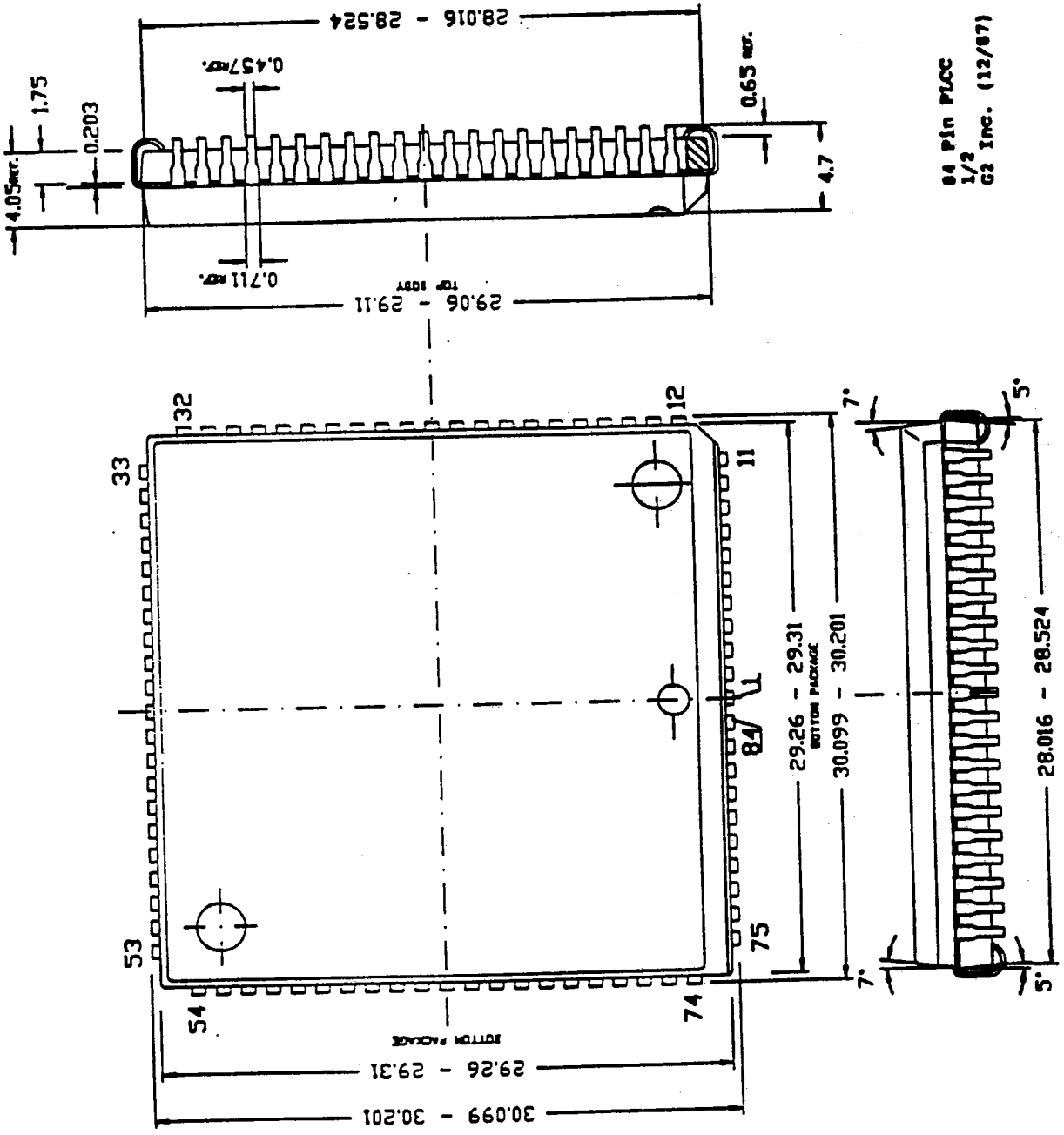
GC101/GC102
Package Outlines



160 Plastic Flat Pack
2/2
G2 Inc. (12/87)

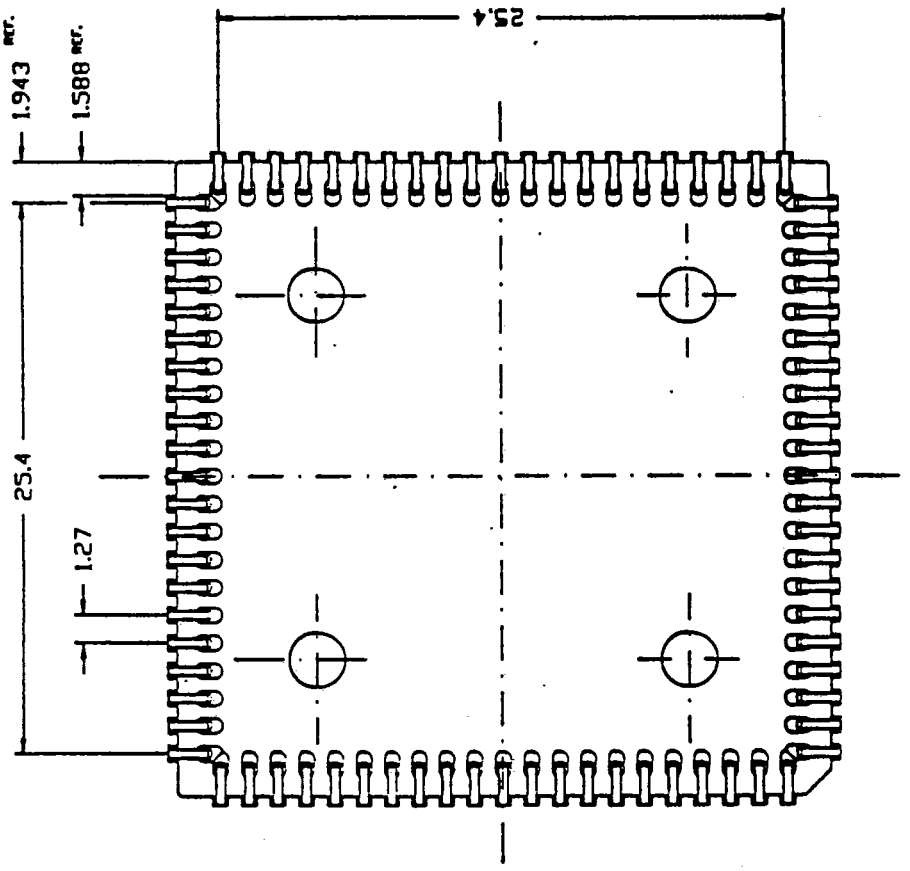


GC101/GC102
Package Outlines

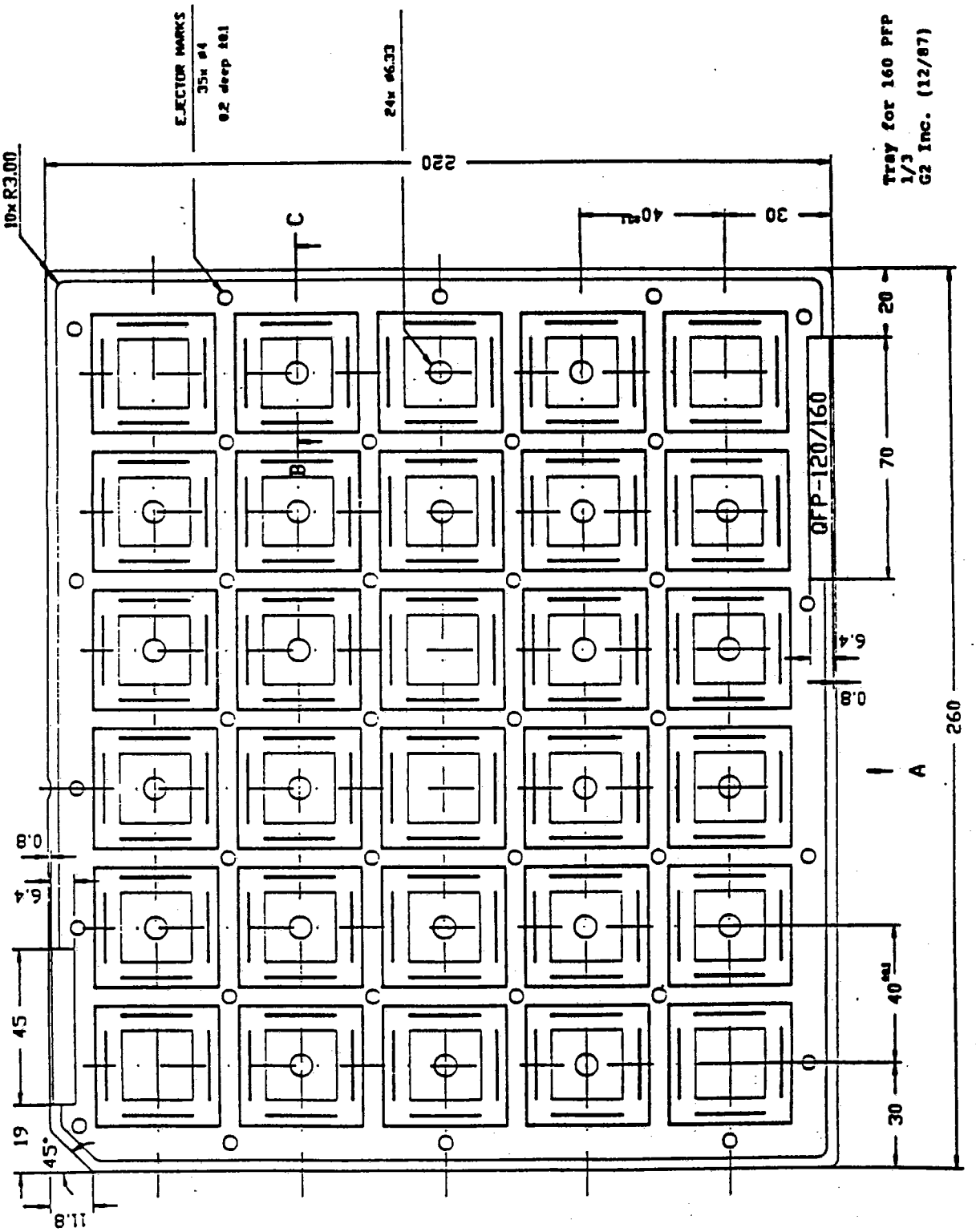


GC101/GC102
Package Outlines

84 Pin PLCC
2/2
G2 Inc. (12/87)



GC101/GC102
Manufacturing Drawings

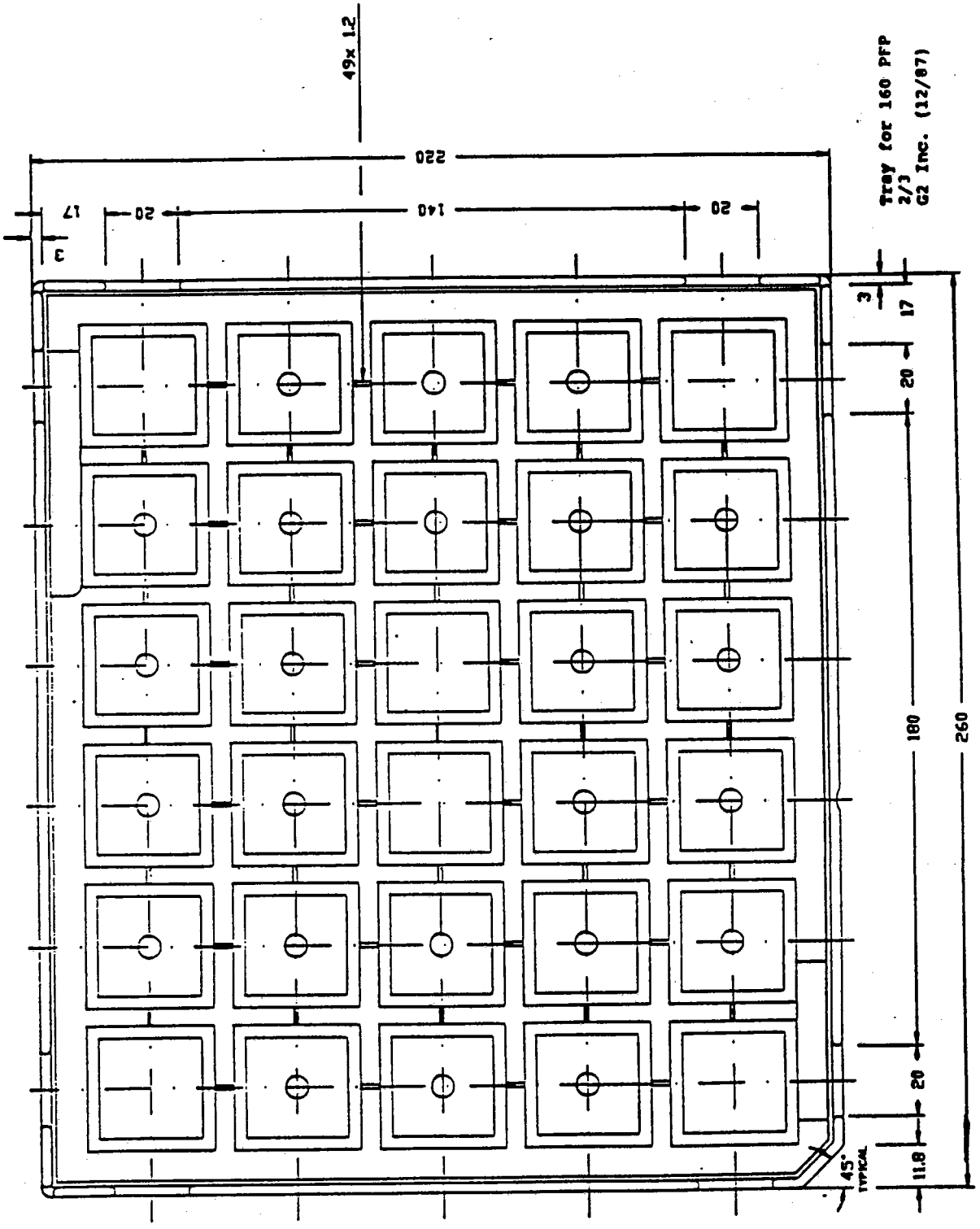


4/1

G2

GC101/GC102
Manufacturing Drawings

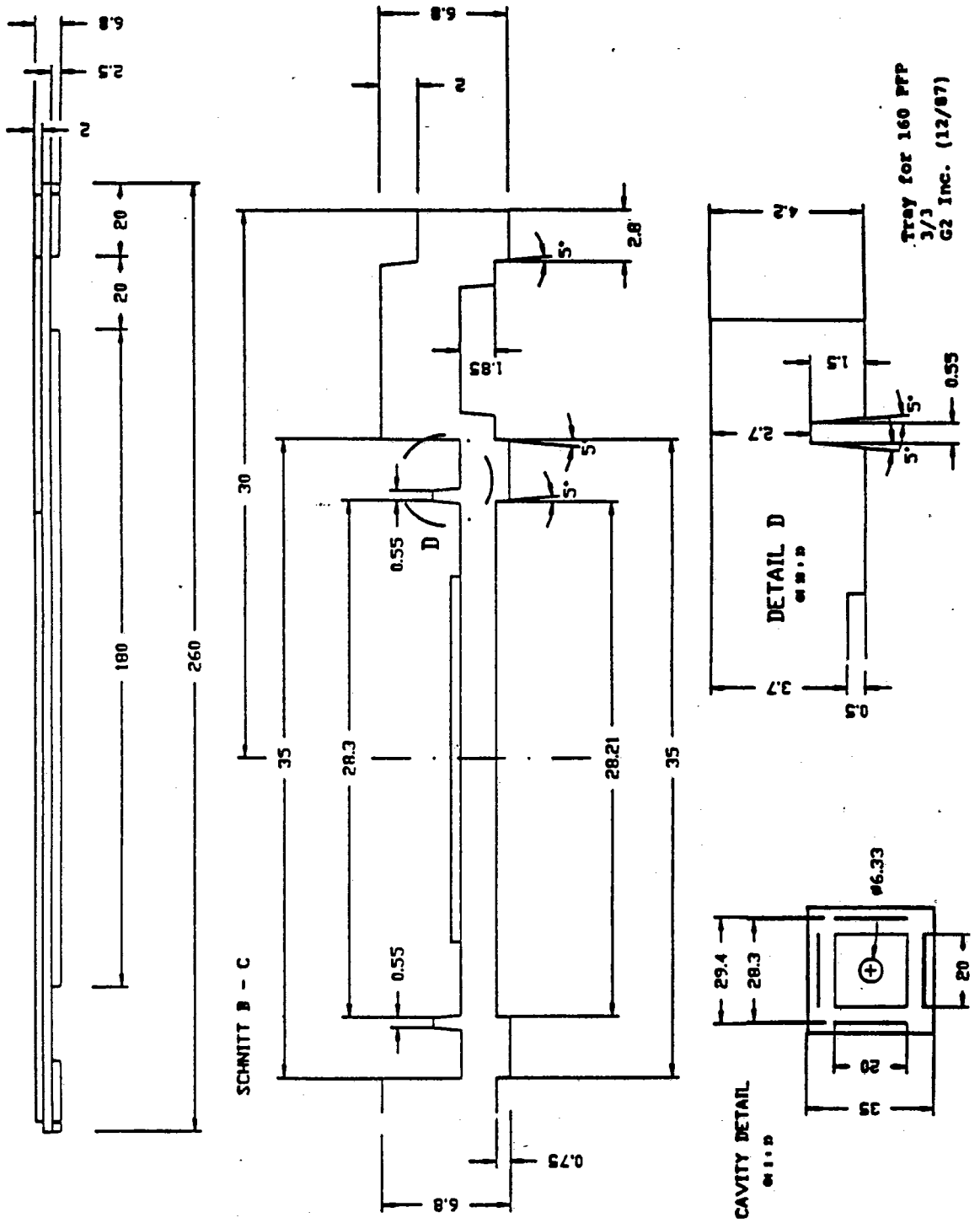
3777475 G-TWO (2) INC 02E 00105 D T-49-17-01



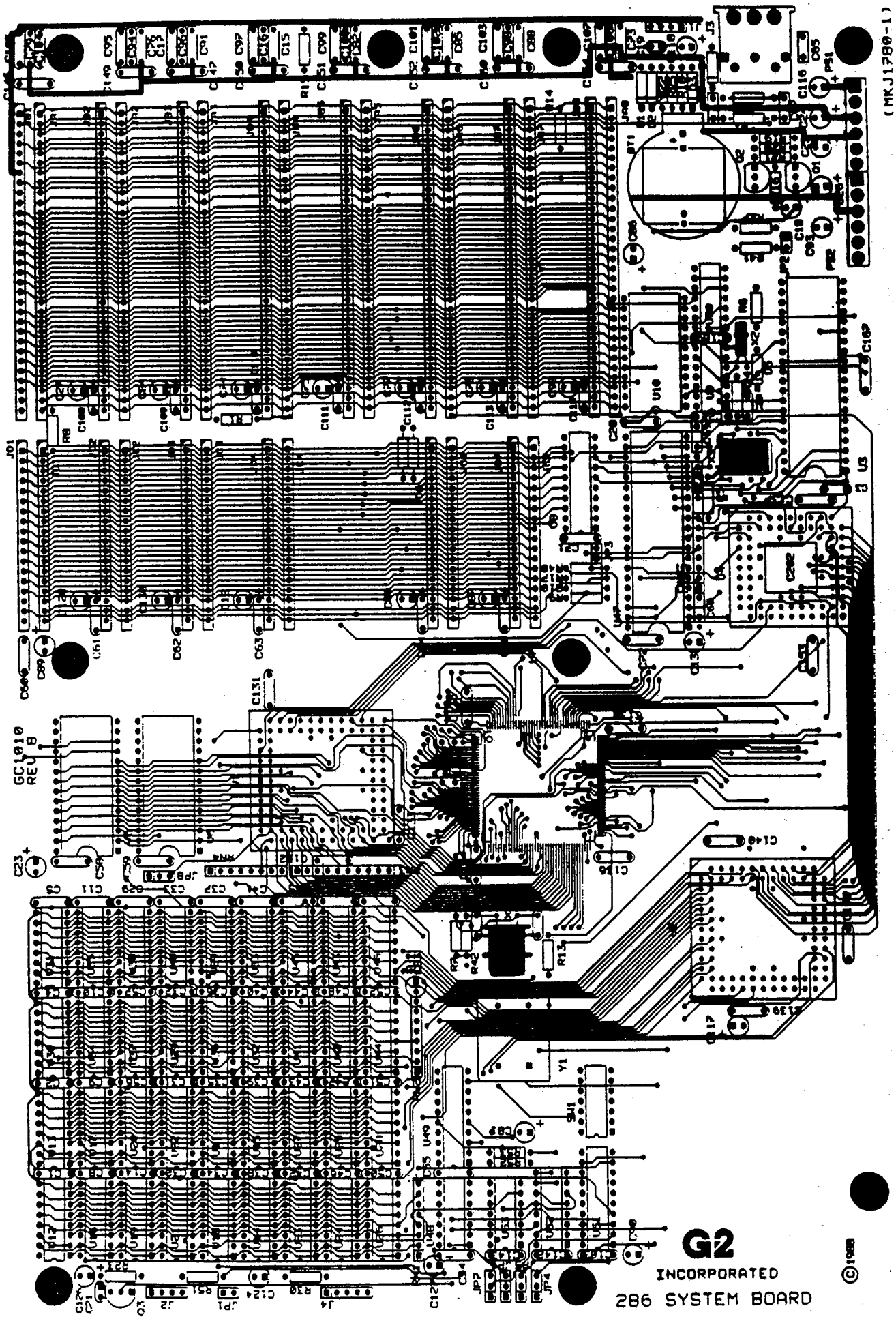
G2

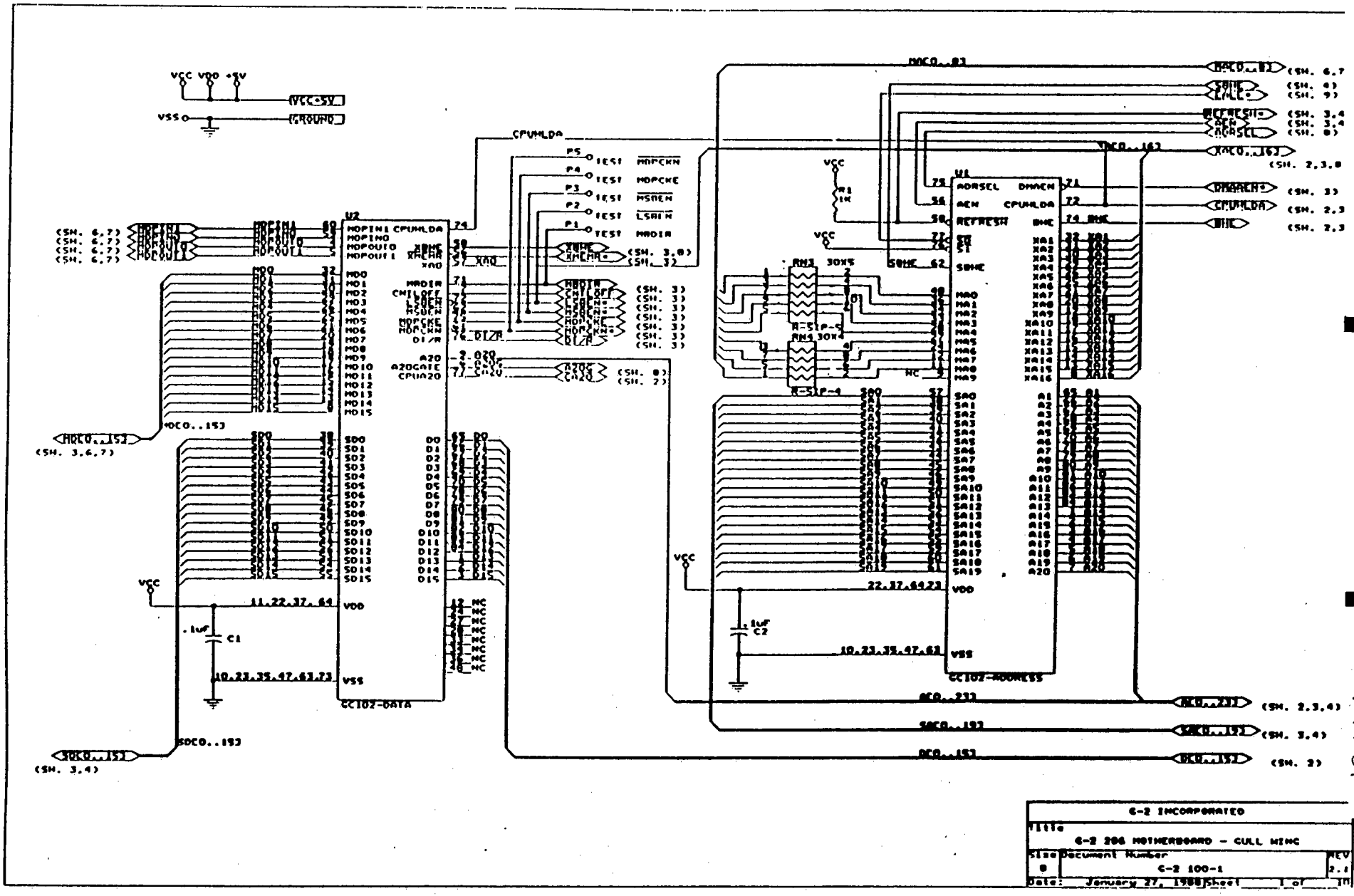
GC101/GC102
Manufacturing Drawings

3777475 G-TWO (2) INC 02E 00106 D T-49-17-01



4/3


(MKJ1780-1)
GC1010
REV B
G2
INCORPORATED
286 SYSTEM BOARD
©1988
G2 INCORPORATED
286 SYSTEM BOARD
LAYER 1 COMPONENT SIDE



G-2 INCORPORATED		
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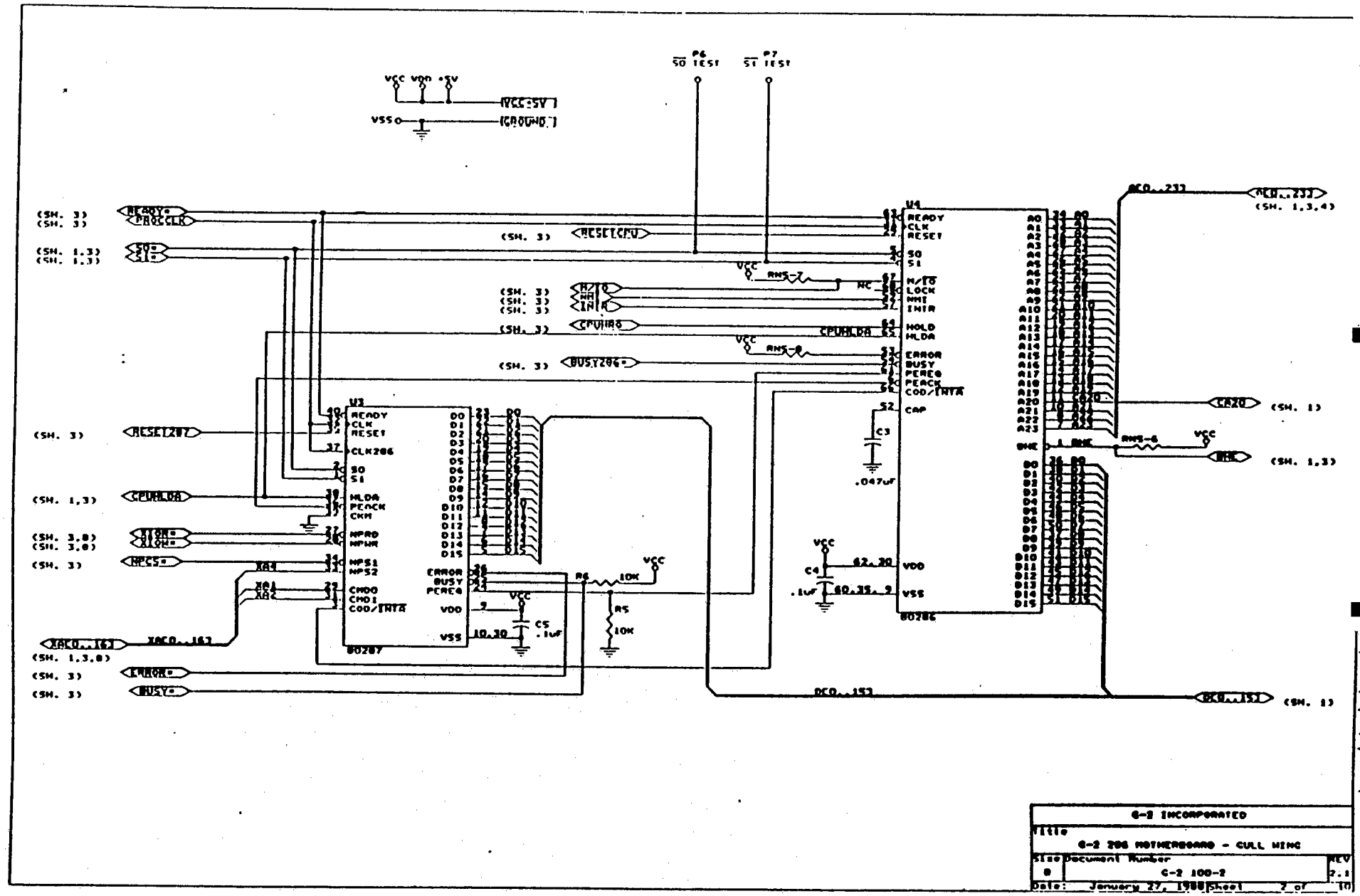
Size: B	Document Number: C-2 100-1	REV: 2.1
Date: January 27, 1988	Sheet 1 of 1	



G-2 INCORPORATED		
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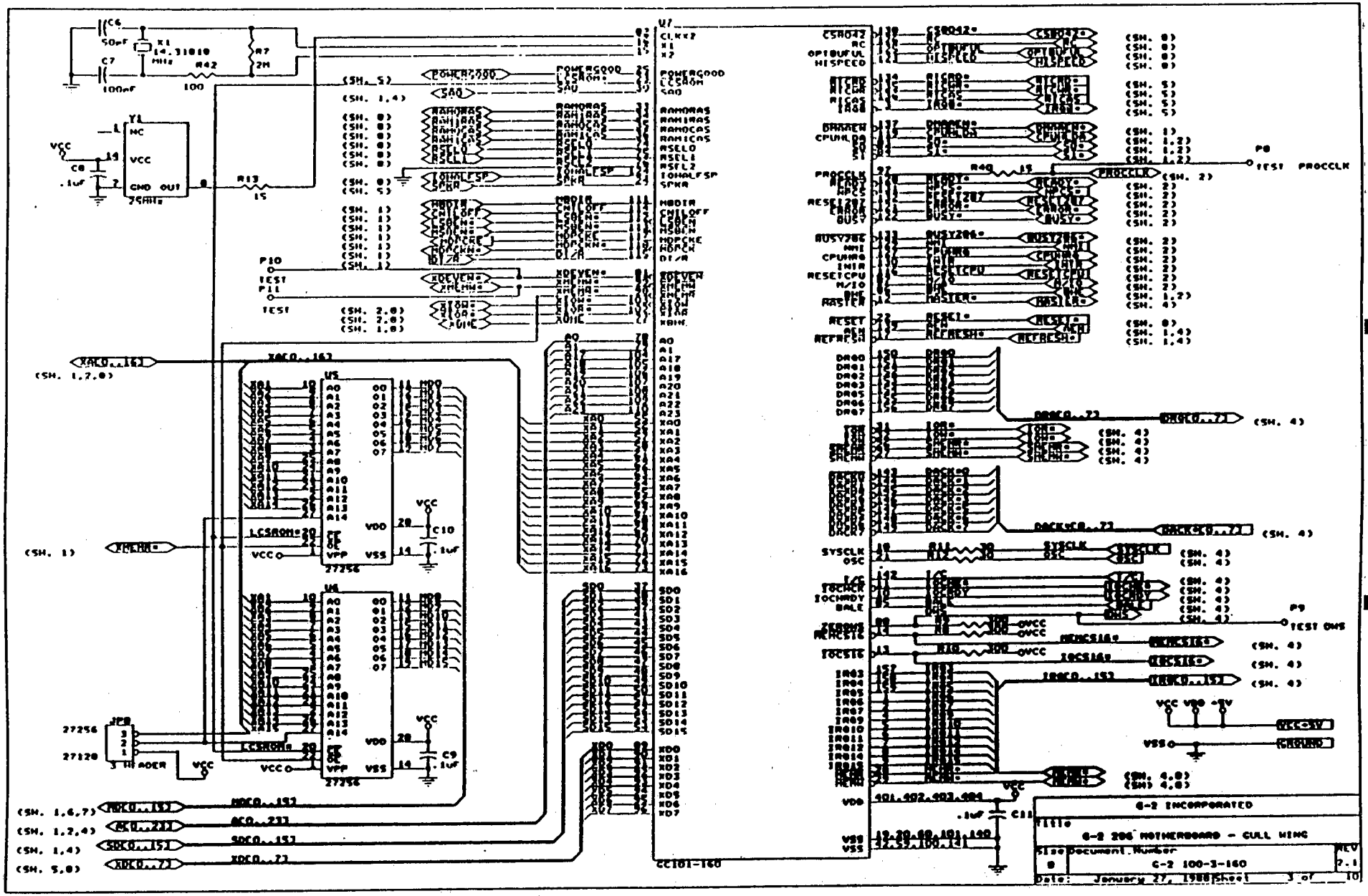
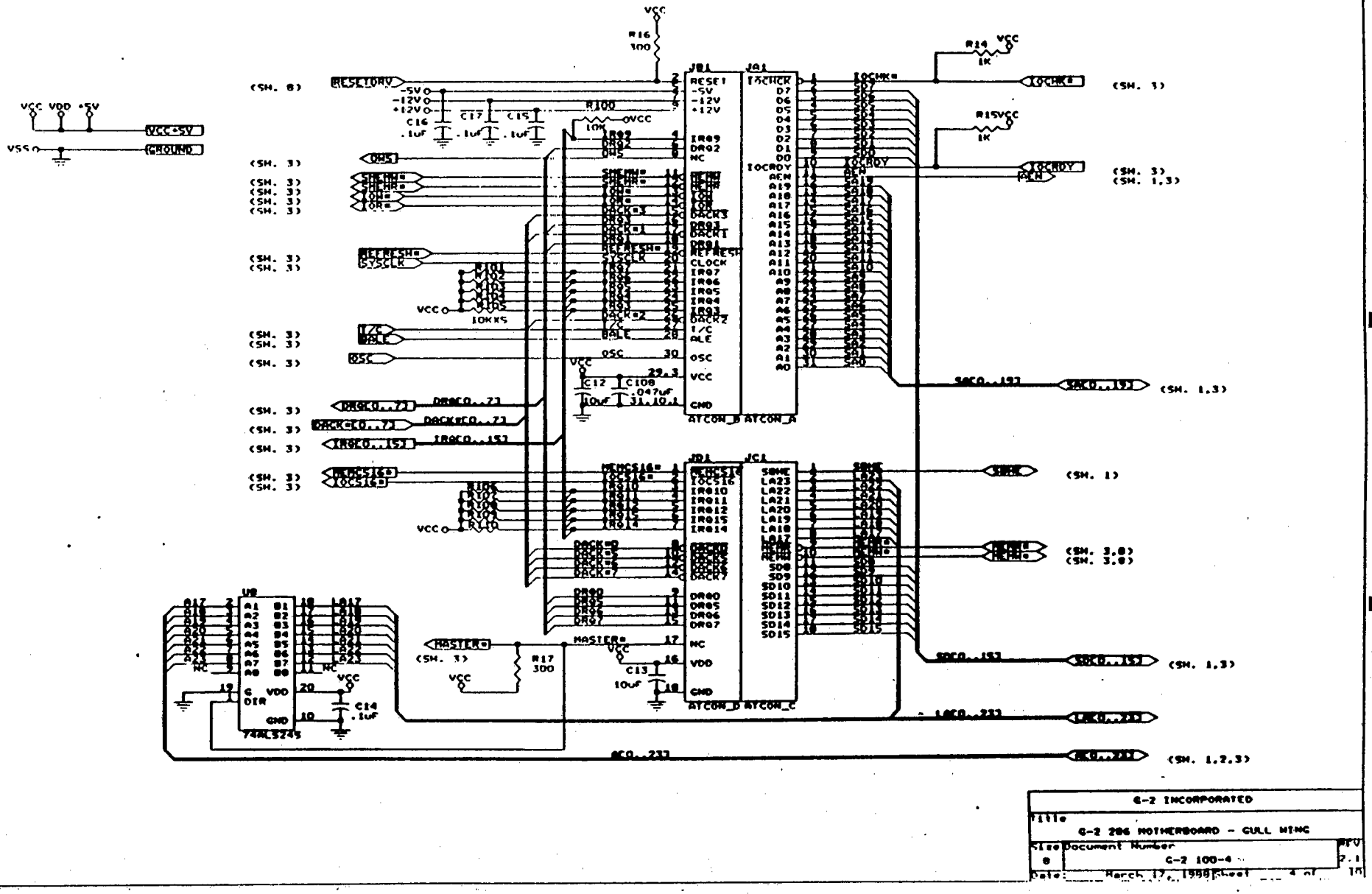
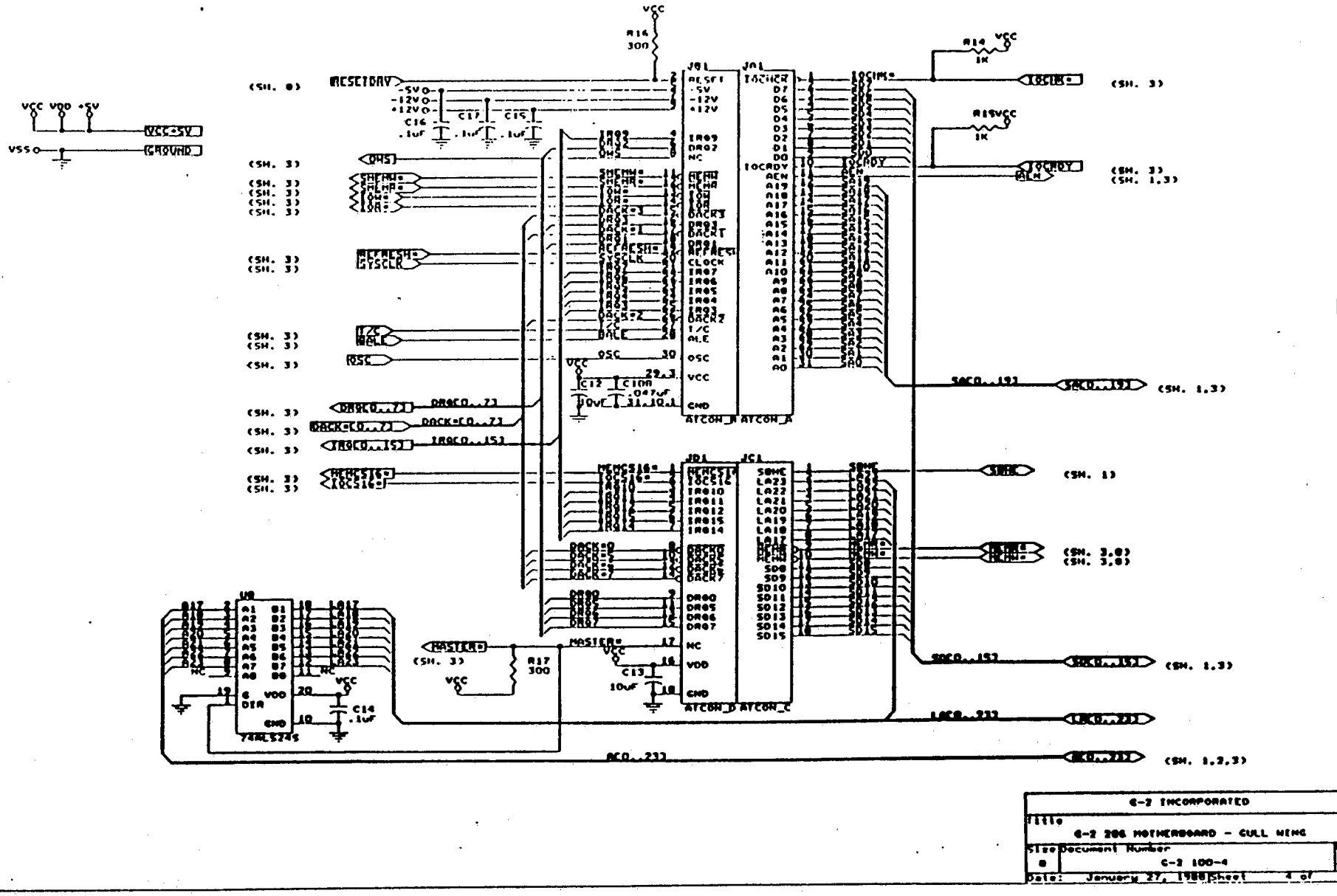
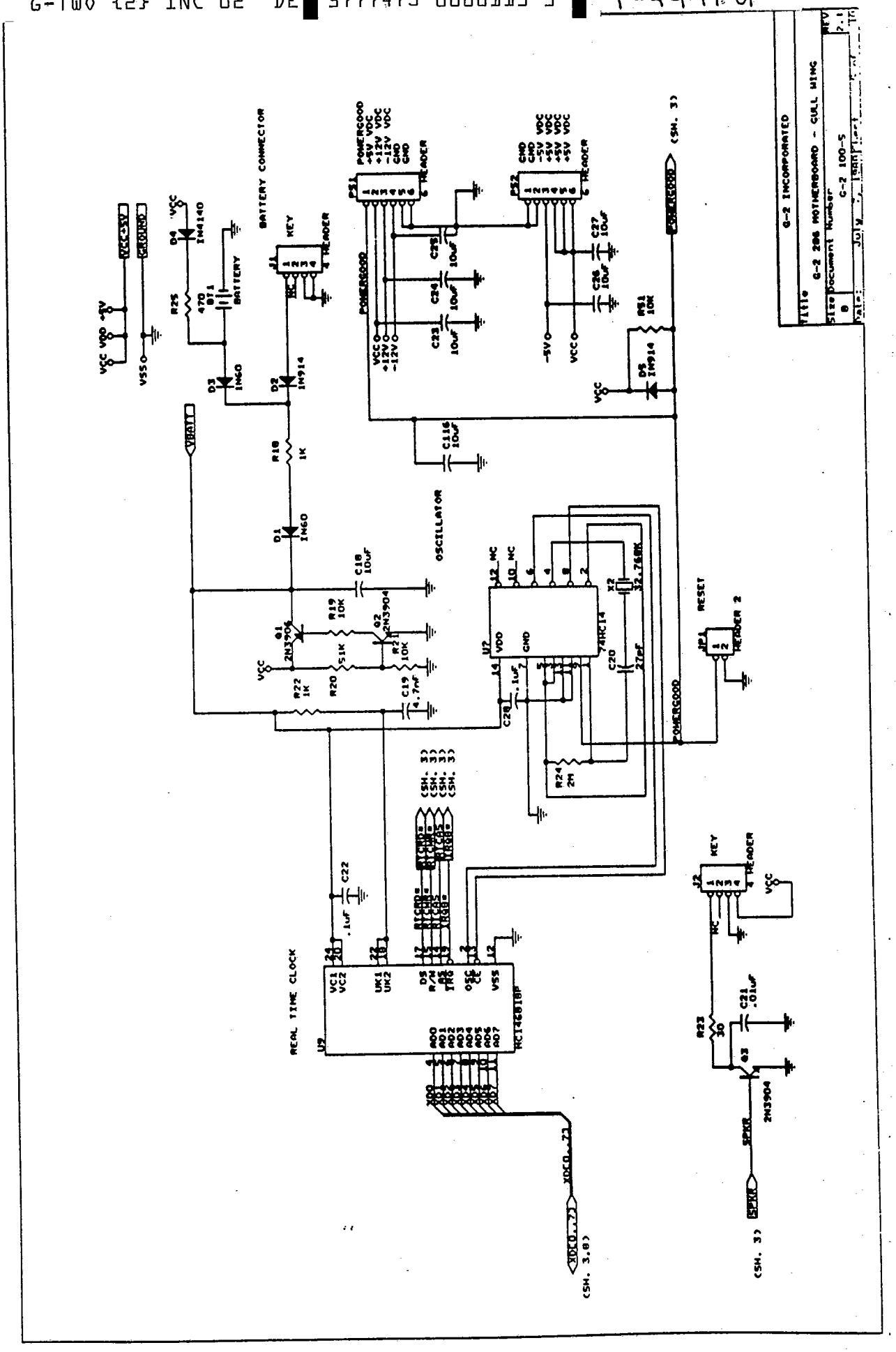
Size: B	Document Number: G-2 100-2	REV: 2.1
Date: January 27, 1988	Sheet 2 of 10	

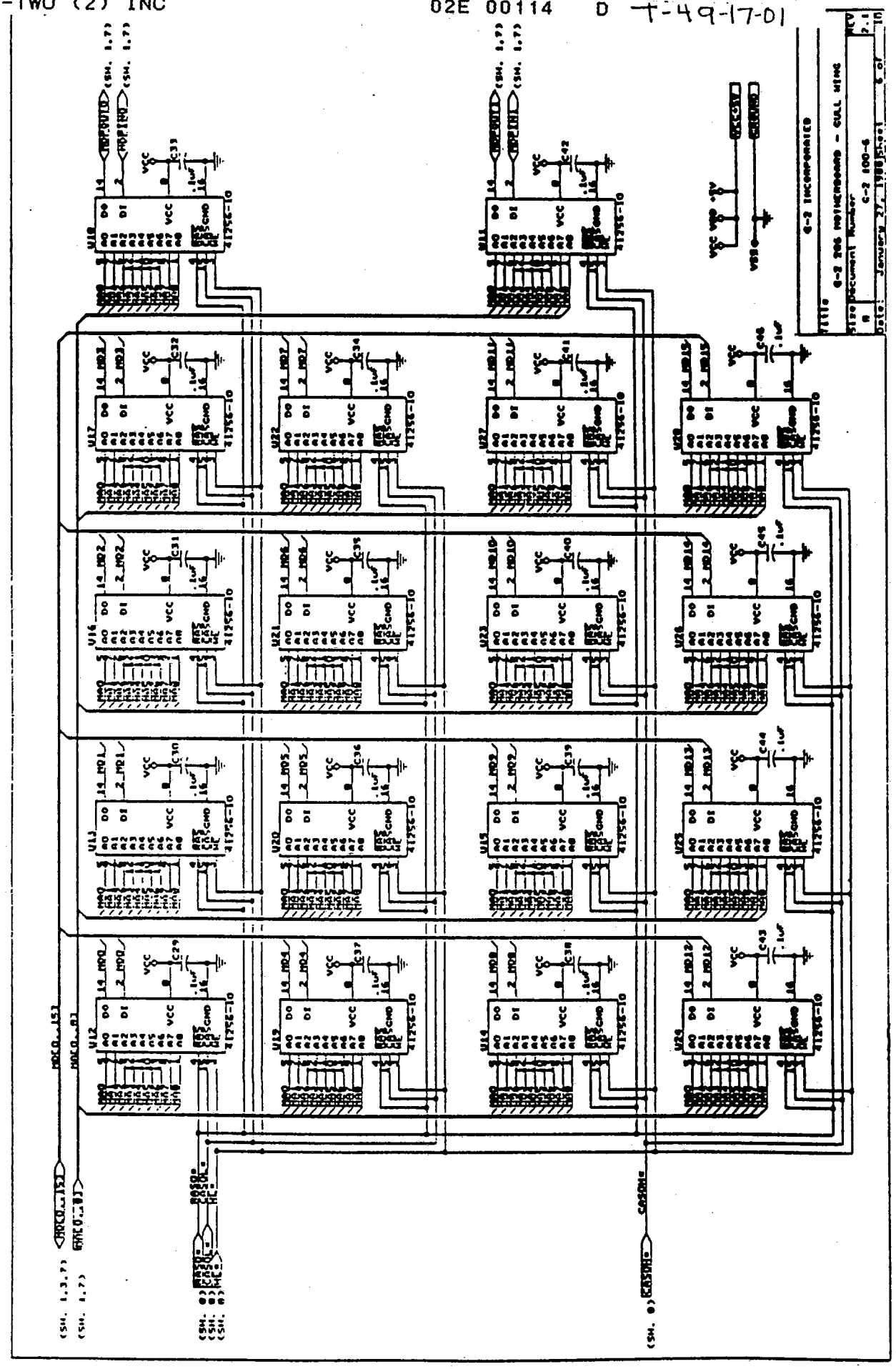


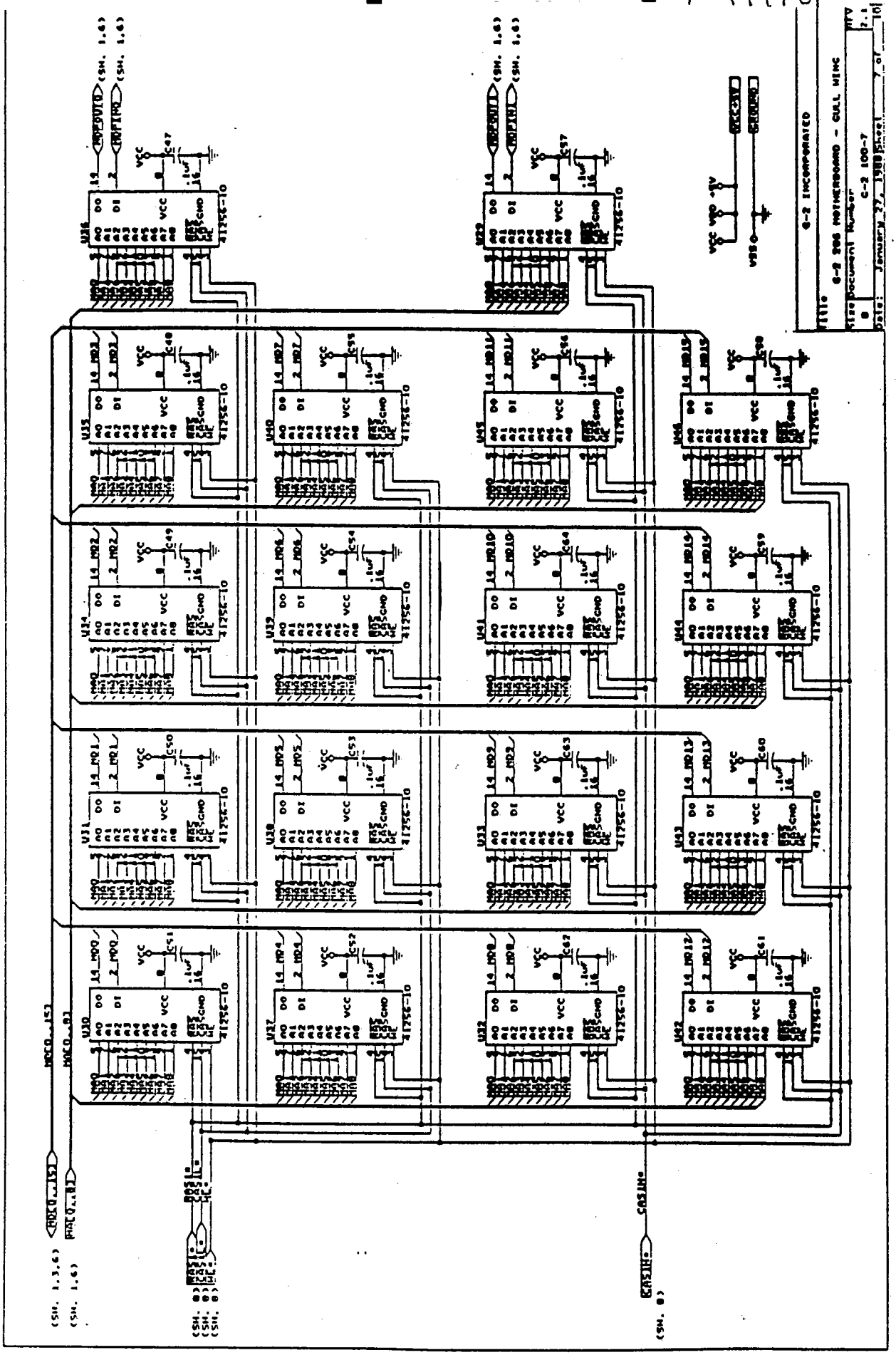


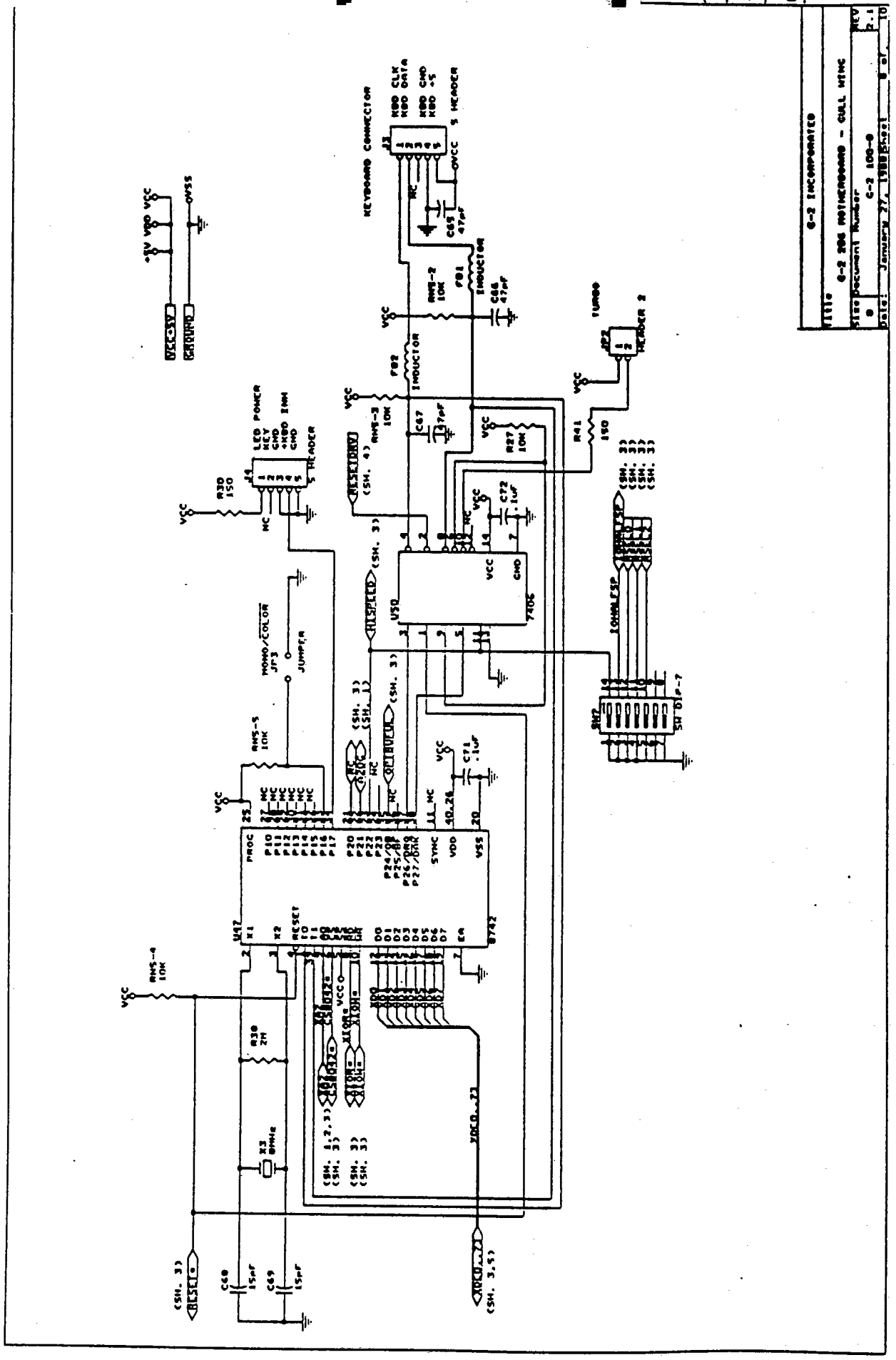
G-2 INCORPORATED		
Title: G-2 286 MOTHERBOARD - GULL WING		
Size: B	Document Number: G-2 100-4	REV: 2.1
Date: March 17, 1988	Sheet 4 of 10	

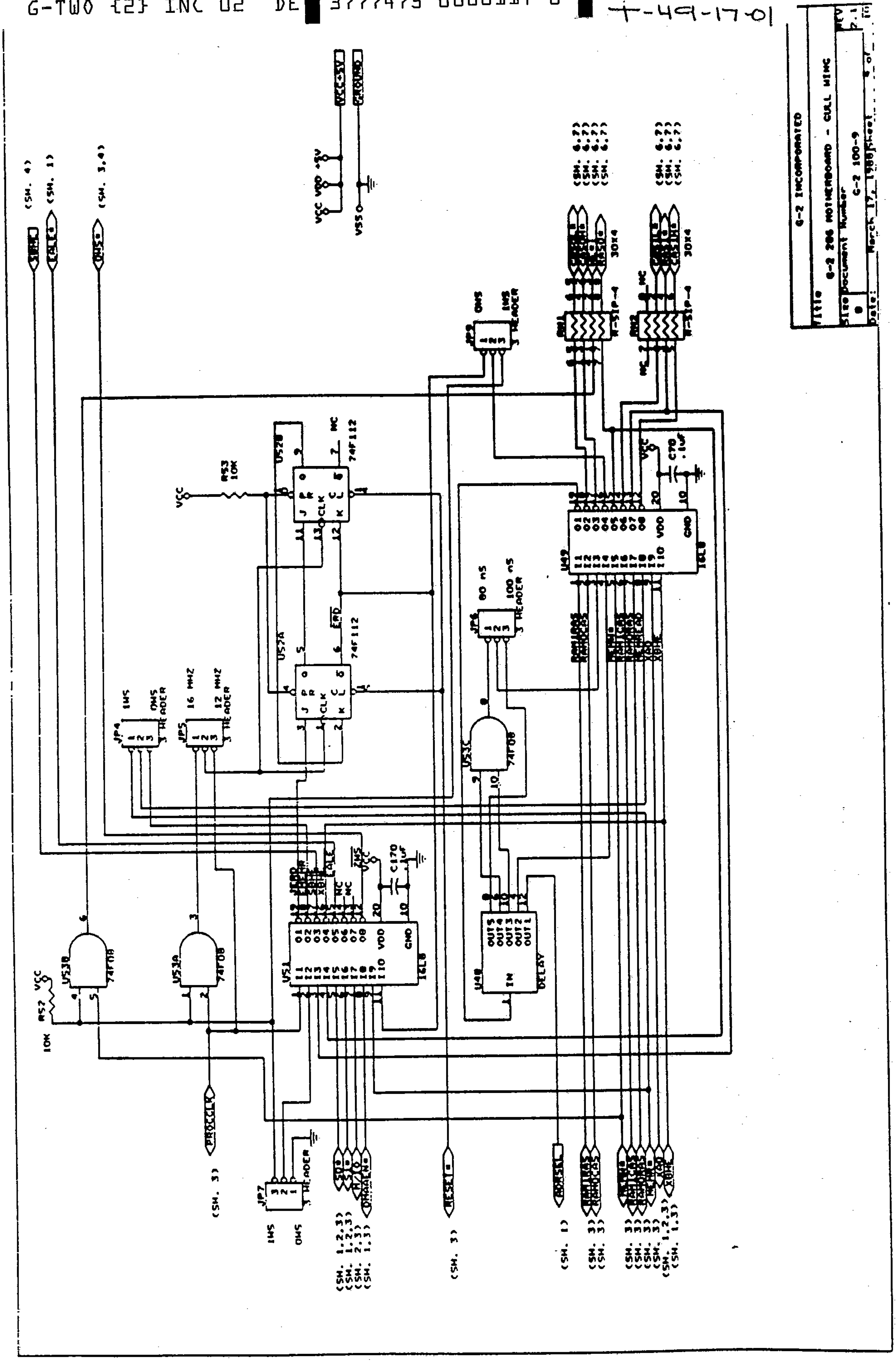



G-2 INCORPORATED
G-2 286 MOTHERBOARD - GULL WING
G-2 100-S
BATTERY CONNECTOR
KEY
HEADER
POWERGOOD
OSCILLATOR
RESET
REAL TIME CLOCK
74HC14
HC146818P
2N3904
VCC
VSS
VBAT
VCC5V
GROUND
SPKR




G-2 INCORPORATED
G-2 386 MOTHERBOARD - CALL MING
C-2 100-7
January 27, 1988
VCC VBB +5V
VSS
GROUND
MCA0..15
MRA0..8
RASL0
RASL1
CASL0
CASL1
CASH0
CASH1


G-2 INCORPORATED
G-2 286 MOTHERBOARD - GULL WING
G-2 100-0
KEYBOARD CONNECTOR
KBD CLK
KBD DATA
KBD GND
KBD +5
+5V VDD VCC
GROUND
LED POWER
KEY
GND
+KBD INH
GND
HEADER
TURBO
HEADER 2
MONO/COLOR
JP3
JUMPER
RESET
HISPEED
OCTRUCK
VCC
GND
SYNC
VDD
VSS
RESET
INDUCTOR
CRYSTAL
HEADER 5X2


G-2 INCORPORATED
G-2 286 MOTHERBOARD - GULL WING
Document Number
G-2 100-9
March 17, 1988
74F112
74F08
16L8
DELAY
R-SIP-4
3 HEADER
VCC VDD +5V
VSS
PROCCLK
RESET
ADDRSEL

55

PAL Equations

```
PAL16L8
U49 RAS and CAS Generation
(C) G2 INC.
rev 4/12/88

RAM1RAS RAM0CAS RAS6080 RAS40  MEMW  RAM1CAS RAM0RAS EMEMR  XA0  GND
XBHE    /CAS1H  /RAS1   /CAS1L /RAS0 ERD     /CAS0H  /CAS0L /RAS VCC

RAS=EMEMR*MEMW*ERD

RAS0=RAM0RAS*/EMEMR*/RAS40
+    RAM0RAS*/MEMW*/RAS40
+    RAM0RAS*/EMEMR*/RAS6080
+    RAM0RAS*/MEMW*/RAS6080
+    RAM0RAS*/ERD

RAS1=RAM1RAS*/EMEMR*/RAS40
+    RAM1RAS*/MEMW*/RAS40
+    RAM1RAS*/EMEMR*/RAS6080
+    RAM1RAS*/MEMW*/RAS6080
+    RAM1RAS*/ERD

CAS0L=/XA0*RAS40*RAM0CAS*/EMEMR
+     /XA0*RAS40*RAM0CAS*/MEMW

CAS1L=/XA0*RAS40*RAM1CAS*/EMEMR
+     /XA0*RAS40*RAM1CAS*/MEMW

CAS0H=/XBHE*RAS40*RAM0CAS*/EMEMR
+     /XBHE*RAS40*RAM0CAS*/MEMW

CAS1H=/XBHE*RAS40*RAM1CAS*/EMEMR
+     /XBHE*RAS40*RAM1CAS*/MEMW
```

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PAL16L8
U51 Early read and Zero wait state generator
(C) G2 INC.
Rev 5/03/88

PRCK ZWSEL RAS1 RAS0 S0 S1 MIOL DMAENL MEMR GND
ERD /ZWS   NC13 NC14 /EALE /XBHE /SBHE /EMEMR /JERD VCC

JERD=S1
+    /S0
+    /MIOL
+    ZWSEL

EMEMR=/ERD
+     /MEMR

EALE=/S0*PRCK
+    /S0*EALE
+    /S1*PRCK
+    /S1*EALE
+     EALE*/PRCK

IF(/DMAENL) SBHE = XBHE

IF(/ZWSEL*DMAENL)ZWS=/RAS0*EMEMR
+                    /RAS1*EMEMR
```