dream

SAM9407

INTEGRATED SOUND STUDIO

- Single chip sound studio, typical application includes :
  - wavetable synthesis, serial MIDI in & out, MPU-401 (UART)
  - game compatible synthesis, with Adlib interface
  - effects : reverb + chorus
  - direct sound : up to 16 simultaneous tracks
  - MOD support
  - 3D with intensity control
  - Equalizer : 4 bands
  - Mixer
- High quality wavetable synthesis
  - 16 bits samples, 44.1 KHz sampling rate
  - Internal computations on 28 bits, DAC support up to 20 bits
  - Alternate loop, 24dB digital filter for each voice
- Professional effects
  - 13 delay lines for resonance free stereo reverb
- Direct sound exceeds Microsoft specification :
  - 7 stereo tracks play + stereo record simultaneous
  - Dynamic filter, amplitude, pitch, four channels pan on each sound track allow dynamic 3D positioning
- Four bands final equalizer allows dramatic sound presence improvement
- Expandable
  - Minimum system : SAM9407 + 512 Kbytes ROM + 32kx8 RAM + Codec
  - Maximum system : SAM9407 + 64 Mbytes DRAM + Codec + DAC
- High performance
  - RISC structure for sound synthesis/processing
  - CISC structure for host communication and house-keeping
  - Audio transfer at maximum 16 bits ISA bus speed
  - Audio transfer in burst mode : removes DMA controlled transfer burden
- Fully programmable
  - Firmware down-loaded to memory at power-up. Easy software upgrade.
  - Chip programming open to third party software companies
  - Powerful programming and debugging tools : algorithm compiler, sound editor, assembler, source debugger. Direct development from PC environment, no special emulator required.
- Top technology
  - Single low frequency crystal operation & built-in PLL minimize RFI
  - TQFP144 space saving package

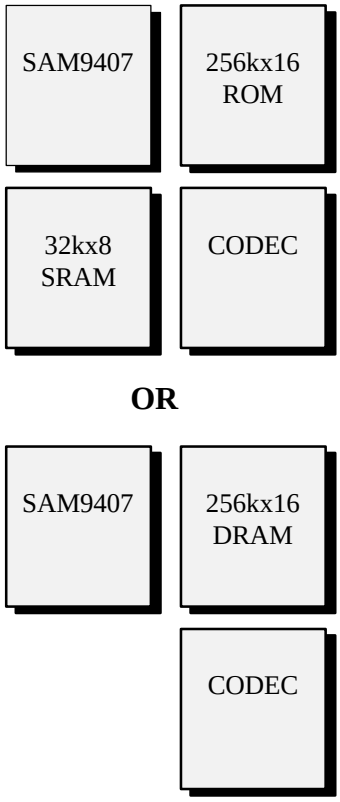
GENERAL MIDI

dream sound inside

Objective specification Feb. 1996

1- TYPICAL DESIGNS

1-1- LOWEST COST



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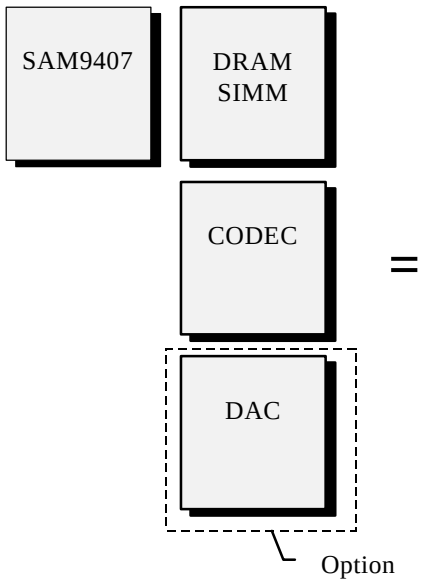
- √ **General Midi compliant wavetable synthesis**
- √ **Compatible reverb + chorus**
- √ **Wave play and record (one stereo channel)**
- √ **Game compatible synthesis**
- √ **3D effect**
- √ **4 bands equalizer**

1-2- TYPICAL



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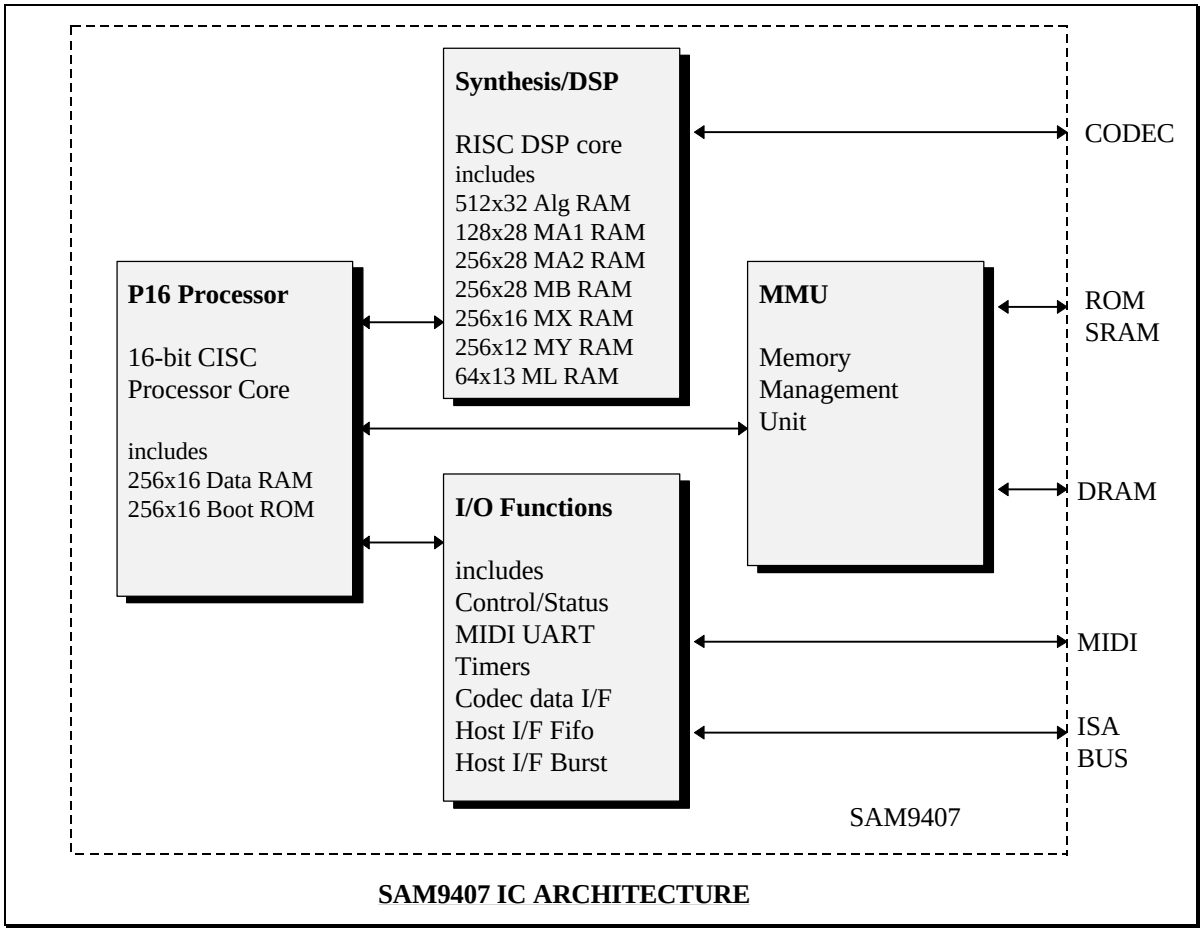
- √ **Professional quality General Midi compliant synthesis**
- √ **GS sound extensions**
- √ **Additional top quality drumsets & bass**
- √ **GS compatible reverb + chorus**
- √ **Downloadable sounds**
- √ **Wave play and record (direct sound) up to 8 stereo channels with dynamic 3D positioning**
- √ **Game compatible synthesis**
- √ **MOD player support**
- √ **3D effect**
- √ **4 channels surround (option)**
- √ **4 bands equalizer**
- √ **Monitor output (option)**

2- GENERAL DESCRIPTION



SAM9407 IC ARCHITECTURE

The highly integrated architecture from SAM9407 combines a specialized high-performance RISC-based digital signal processor (Synthesis/DSP) and a general purpose 16 bits CISC-based control processor on a single chip. An on-chip memory management unit (MMU) allows the synthesis/DSP and the control processor to share external ROM and/or RAM memory devices. An intelligent peripheral I/O interface function handles other I/O interfaces, such as the ISA PC bus, the on-chip MIDI UART, and the Codec control interface, with minimum intervention from the control processor.

Synthesis/DSP engine

The synthesis/DSP engine operates on a frame timing basis with the frame subdivided into 64 processes slots. Each process is itself divided into 16 micro-instructions known as « algorithm ». Up to 32 synthesis/DSP algorithms can be stored on-chip in the Alg RAM memory, allowing the device to be programmed for a number of audio signal generation/processing applications. The synthesis/DSP engine is capable of generating 64 simultaneous voices using algorithms such as wavetable synthesis with interpolation, alternate loop and 24dB resonant filtering for each voice. Slots may be linked together (ML RAM) to allow implementation of more complex synthesis algorithms.
A typical multimedia application will use half the capacity of the synthesis/DSP engine for synthesis, thus providing state of the art 32 voices wavetable polyphony. The remaining processing power will be used for typical function like reverberation, chorus, direct sound, 3D effect, equalizer, etc.

Frequently accessed synthesis/DSP parameter data are stored into 5 banks of on-chip RAM memory. Sample data or delay lines, which are accessed relatively infrequently are stored in external ROM, SRAM or DRAM memory. The combination of localized micro-program memory and localized parameter data allows micro-instructions to execute in 20 ns (50 MIPS). Separate busses from each of the on-chip parameter RAM memory banks allow highly parallel data movement to increase the effectiveness of each micro-instruction. With this architecture, a single micro-instruction can accomplish up to 6 simultaneous operations (add, multiply, load, store, etc.), providing a potential throughput of 300 million operations per second (MOPS).

P16 control processor and I/O functions

The P16 control processor is a general purpose 16-bit CISC processor core, which runs from external memory. A Boot/Macro ROM is included on-chip to accelerate commonly executed routines and to allow the use of RAM only devices for the external memory. The P16 includes also 256 words of local RAM data memory.

The P16 control processor writes to the parameter RAM blocks within the synthesis/DSP core in order to control the synthesis process. In a typical application, the P16 control processor parses and interprets incoming commands from the MIDI UART or from the PC ISA interface and then controls the Synthesis/DSP by writing into the parameter RAM banks in the DSP core. Slowly changing synthesis functions, such as LFOs, are implemented in the P16 control processor by periodically updating the DSP parameter RAM variables.

The P16 control processor interfaces with other peripheral devices, such as the system control and status registers, the on-chip MIDI UART, the on-chip timers and the ISA PC interface through specialized « intelligent » peripheral I/O logic. This I/O logic automates many of the system I/O transfers to minimize the amount of overhead processing required from the P16.

The ISA PC interface is implemented using three address lines (A2, A1, A0), a chip select signal, read and write strobes from the host and a 16 bits data bus (D0-D15). The data bus can drive the PC bus directly (24mA buffers). An external decoder (PAL) or plug & play IC is required to map the 12 bits I/O addresses and AEN from the PC into the 3 address lines and chip select from the SAM9407.
The ISA PC interface supports a byte-wide primary I/O interface, a byte wide auxiliary interface and a 16-bit port dedicated to burst transfers.
The primary I/O interface is normally used to implement a Roland MPU-401 UART-mode compatible interface. It is specified by address A2A1A0=00X, address 000 being the data register, address 001 being the status/control registers. Besides the standard two status bits of the MPU-401, two additional bits are provided to expand the MPU-401 protocol.
The auxiliary interface is allocated the address range A2A1A0=1XX. It is normally used to implement a game compatible interface.
Address A2A1A0=010 specifies a 16 bit I/O port. It is mainly used for burst audio transfers to/from the PC using very efficient PC instructions like REP OUTSW or REP INSW which operate at maximum ISA bus bandwidth. This port may also be used for fast program or sound bank uploads.

Memory Management Unit (MMU)

The Memory Management Unit (MMU) block allows external ROM and/or RAM memory resources to be shared between the synthesis/DSP and the P16 control processor. This allows a single device (i.e. DRAM) to serve as sample memory storage / delay lines for the synthesis/DSP and as program storage / data memory for the P16 control processor.

3- PIN DESCRIPTION

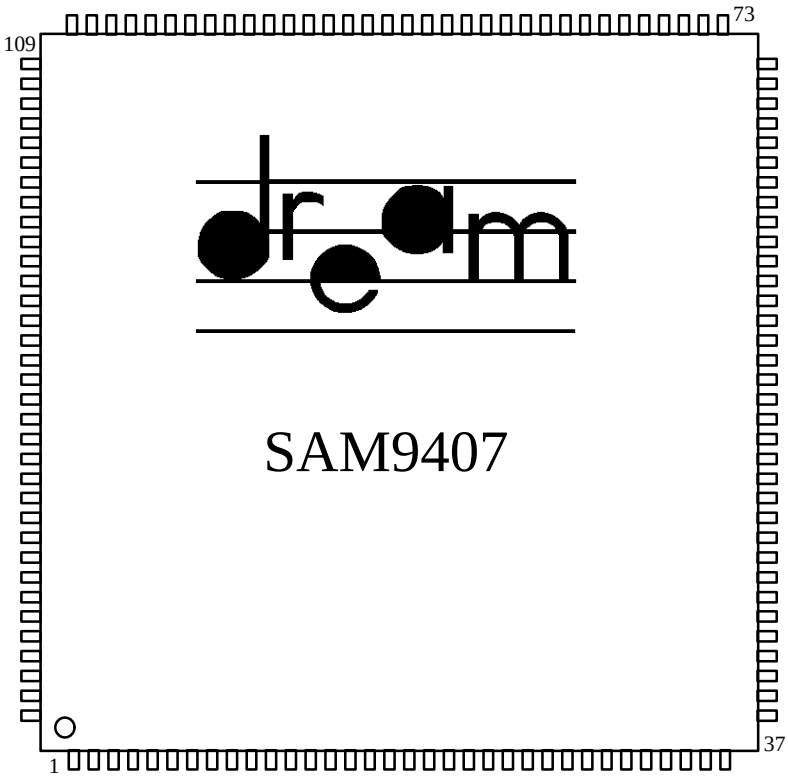
3-1- PIN BY FUNCTION

name	pin #	type	
GND	17	PWR	Power ground - all GND pins should be returned to digital ground
VC3	3	PWR	Core power +5V +/-5% all VC3 pins should be returned to +5V. Layout provisions should be done for future releases of the chip with 3.3V VC3.
VCC	15	PWR	Power +5V +/- 5% - all VCC pins should be returned to +5V
D0-D15	16	I/O	16 bit data bus to host processor. Has enough driving power to drive PC bus directly (24mA buffer). Information on these pins are : - parallel MIDI (MPU-401 type applications) - Adlib control (game sound type emulation) - Down/up-load of PCM data or application programs
CS/	1	IN	Chip select from host, active low.
WR/	1	IN	Write from host, active low.
RD/	1	IN	Read from host, active low.
A0-A2	3	IN	Selects one of 8 internal registers 0,1 : MPU-401 registers 2,3 : 16 bit data (burst DMA mode) 4,7 : game sound registers
IRQ	1	TSout	Tri-state output pin. Can be connected directly to host IRQ line (24mA).
SBHE/	1	IN	Bus high enable signal from the host (active low).
I/0 READY	1	OUT	Open drain output buffer (24mA) ; driven low during 16 bits burst mode transfers to synchronize PC to the SAM9407 memory.
I/O CS16/	1	OUT	Open drain output buffer (24mA); driven low during 16 bits burst mode transfers. Indicates to host that a 16 bit I/O is in progress.
RESET/	1	IN	Master reset input, active low. Schmidt trigger input.
X1,X2	2	-	Crystal connection. Crystal frequency should be Fs*256 (typ 12.288 MHz) Xtal frequency is internally multiplied by 4 to provide the IC master clock. X1 can also be used as external clock input, X2 as clock output. The X2 signal frequency is compatible with most oversampling DACs/Codecs
DABD0-1	2	OUT	Two stereo serial audio data output (4 audio channels). Each output holds 64 bits (2x32) of serial data per frame. Audio data has up to 20 bits precision. DABD0 can hold additional control data (mute, A/D gain, D/A gain, etc.) directly compatible with CS4216/CS4218
CLBD	1	OUT	Audio data bit clock, provides timing to DABD0-1.
WSBD	1	OUT	Audio data word select. The timing of WSBD can be selected to be I2C or Japanese compatible.
DAAD	1	IN	Stereo serial audio data input.
MIDI IN	1	IN	TTL level MIDI IN input
MIDI OUT	1	OUT	TTL level MIDI OUT output
WA0-24	25	OUT	External memory address (ROM/SRAM). Up to 32 Mega words (64 Mega 8 bit samples).
WD0-15	16	I/O	PCM ROM/SRAM/DRAM data
RBS	1	OUT	SRAM byte select : should be connected to the lower RAM address when 8 bit wide SRAM is used. The type of RAM (16bits/8bits) can be selected by program
WCS0/	1	OUT	PCM ROM chip select, active low
WCS1/	1	OUT	SRAM chip select, active low
WWE/	1	OUT	SRAM/DRAM write enable, active low. Timing compatible with SIMM DRAM early write feature.
WOE/	1	OUT	PCM ROM/SRAM output enable, active low
BOOT	1	IN	Active high, specifies that built-in CPU bootstrap should be used at power-up (case of DRAM connection only).
DRA0-11	12	OUT	Multiplex DRAM address : 9, 10, 11, 12 bits multiplex addressing can be used (from 256kx16 to 16Mx16 type configurations).
RAS/	1	OUT	DRAM row address strobe
CAS/	1	OUT	DRAM column address strobe
P0-P3	4	I/O	General purpose configurable I/O pins
S0-S1	2	OUT	Indicates type of external memory cycle. S1S0=00:idle, 01:Synthesis access, 10:Instruction fetch, 11:Processor read/write
RUN	1	OUT	High when the synthesis is initialized. Can be used as RESET/ for an external device (CODEC).
LFT	1	ANA	PLL low pass filter : should be connected to an external RC network
TEST0-2	3	IN	Test pins, should be returned to GND.
PDWN/	1	IN	Power down, active low

3-2- PIN-OUT

108	GND	99	RD/	90	WA10	81	WA6
107	D11	98	VCC	89	A0	80	WA5
106	VCC	97	WR/	88	WA9	79	WA4
105	D10	96	WA16	87	WA8	78	WA3
104	WA18	95	WA15	86	WA7	77	GND
103	WA17	94	WA14	85	GND	76	D7
102	A2	93	WA13	84	D9	75	VCC
101	A1	92	WA12	83	VCC	74	D6
100	GND	91	WA11	82	D8	73	WA2

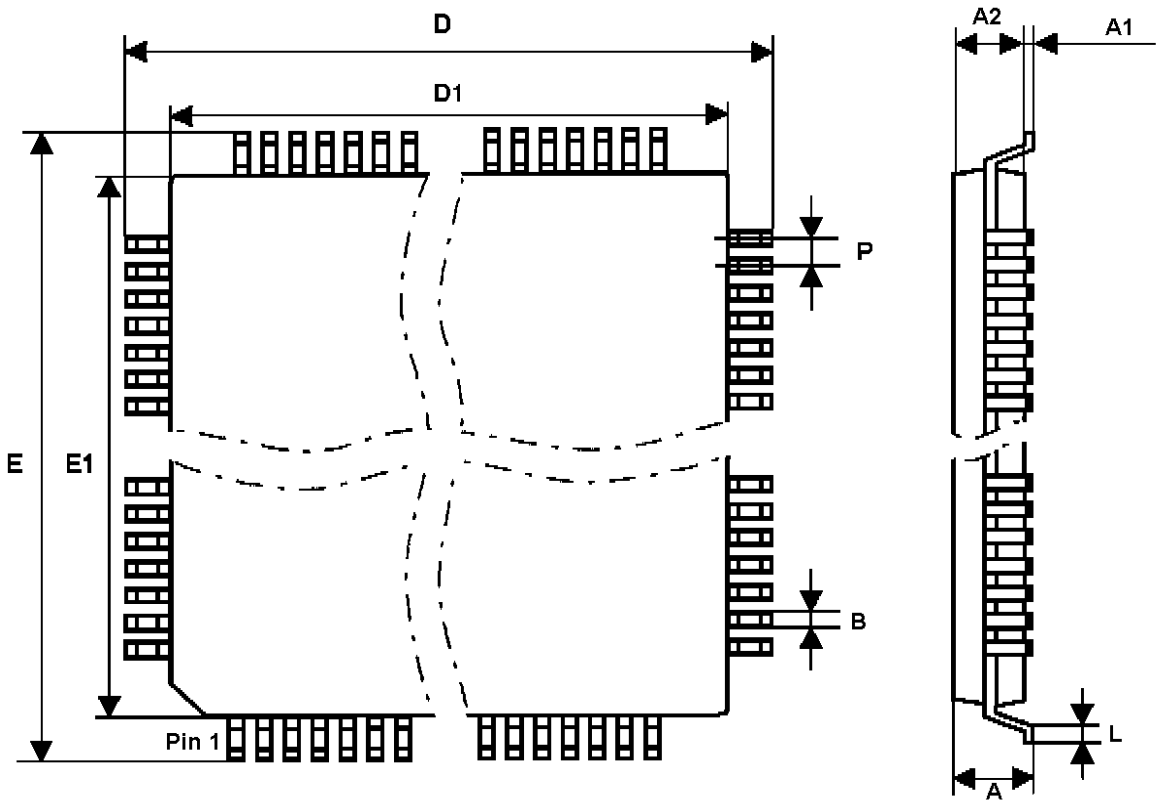
109	WA19	110	D12	111	VC3	112	D13
113	WA20	114	WA21	115	CAS/	116	RAS/
117	WA22	118	VCC	119	GND	120	GND
121	SBHE/	122	WA23	123	WA24	124	WD0
125	WD1	126	WD2	127	I/O READY	128	WD3
129	WD4	130	WD5	131	WD6	132	WD7
133	GND	134	CS/	135	VCC	136	S0
137	WD8	138	WD9	139	S1	140	WD10
141	D14	142	WD11	143	D15	144	WD12



72	WA1	71	D5	70	GND	69	D4
68	VCC	67	DRA11	66	WA0	65	DRA10
64	GND	63	TEST2	62	TEST1	61	TEST0
60	P3	59	P2	58	P1	57	P0
56	GND	55	DRA9	54	VCC	53	WOE/
52	WCS1/	51	WCS0/	50	WWE/	49	WSBD
48	DABD1	47	DRA8	46	DRA7	45	DABD0
44	DRA6	43	DAAD	42	DRA5	41	GND
40	D3	39	VCC	38	D2	37	BOOT

1	VCC	10	WD15	19	RESET/	28	VC3
2	IRQ	11	GND	20	PDWN/	29	GND
3	GND	12	VCC	21	VCC	30	VCC
4	I/O CS16/	13	GND	22	GND	31	GND
5	WD13	14	VC3	23	DRA2	32	D0
6	MIDI OUT	15	VC3	24	DRA3	33	CLBD
7	WD14	16	LFT	25	MIDI IN	34	VC3
8	DRA0	17	X2	26	RUN	35	D1
9	DRA1	18	X1	27	DRA4	36	RBS

3-3- MECHANICAL DIMENSIONS



SAM9407
THIN PLASTIC 144 LEAD QUAD FLAT PACK (TQFP144)

	MIN.	NOM.	MAX.
A	1.40	1.50	1.60
A1	0.05	0.10	0.15
A2	1.35	1.40	1.45
D	21.90	22.00	22.10
D1	19.90	20.00	20.10
E	21.90	22.00	22.10
E1	19.90	20.00	20.10
L	0.45	0.60	0.75
P		0.50	
B	0.17	0.22	0.27

4- ABSOLUTE MAXIMUM RATINGS (All voltages with respect to 0V, GND=0V)

Parameter	Symbol	Min	Typ	Max	Unit
Ambient temperature (Power applied)	-	-40	-	+85	°C
Storage temperature	-	-65	-	+150	°C
Voltage on any pin	-	-0.5	-	VCC+0.5	V
Supply voltage	VCC/VC 3	-0.5	-	6.5	V
Maximum IOL per I/O pin	-	-	-	10	mA

5- RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	VCC	4.5	5.0	5.5	V
Supply voltage (note 1)	VC3	4.5	5.0	5.5	V
Operating ambient temperature	tA	0	-	70	°C

note 1 : Future issues will have VC3 = 3.3V and 5V tolerant I/Os

6- D.C. CHARACTERISTICS (TA=25°C, VCC,VC3=5V±10%)

Parameter	Symbol	Min	Typ	Max	Unit
Low level input voltage	VIL	-0.5	-	0.8	V
High level input voltage	VIH	2.0	-	VCC+0.5	V
Low level output voltage D<15:0>, IRQ, I/O ready : IOL=-24mA others except LFT : IOL=-3.2mA	VOL	-	-	0.45	V
High level output voltage D<15:0>, IRQ, I/O ready : IOH=10mA others except LFT : IOH=0.8mA	VOH	2.4	-	-	V
Power supply current (crystal freq.=12MHz)	ICC	-	50	100	mA
Power down supply current	-		100	150	µA

7- TIMINGS

All timings conditions : Ta=25°C, signals I/O READY, I/O CS16/, D0-D15 with 220 ohms pull-up, 30pF capacitance, signal IRQ with 470 ohms pull-down, 30pF capacitance, all other outputs except X2 and LFT load capacitance=30pF.
All timings refer to tck, which is the internal master clock period.
The internal master clock frequency is 4 times the frequency at pin X1. Therefore tck=txtal/4.
The sampling rate is given by 1/(tck*1024). The maximum crystal frequency/clock frequency at X1 is 12.288 MHz (48 KHz sampling rate).

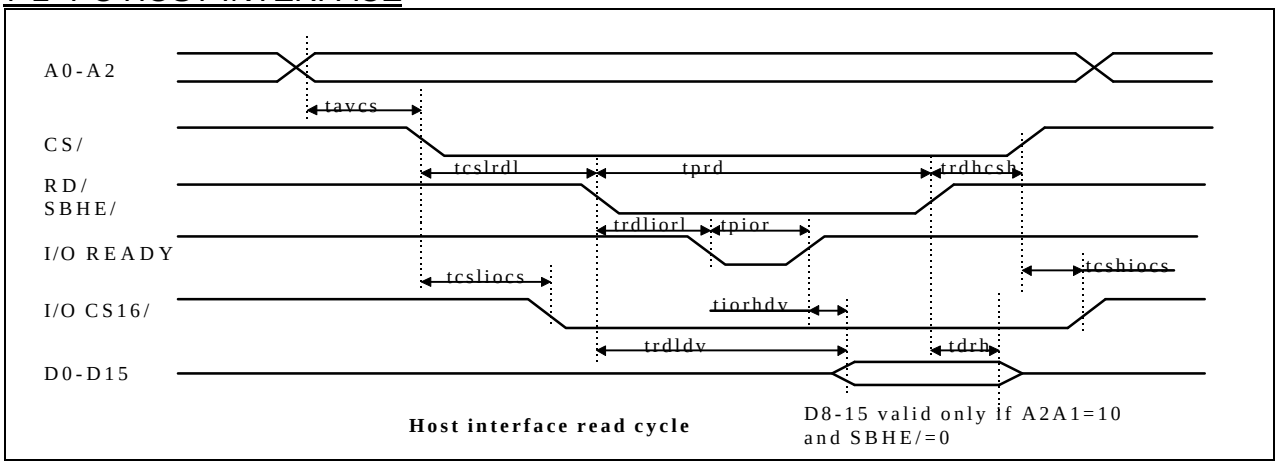
7-1- CRYSTAL FREQUENCY SELECTION CONSIDERATIONS

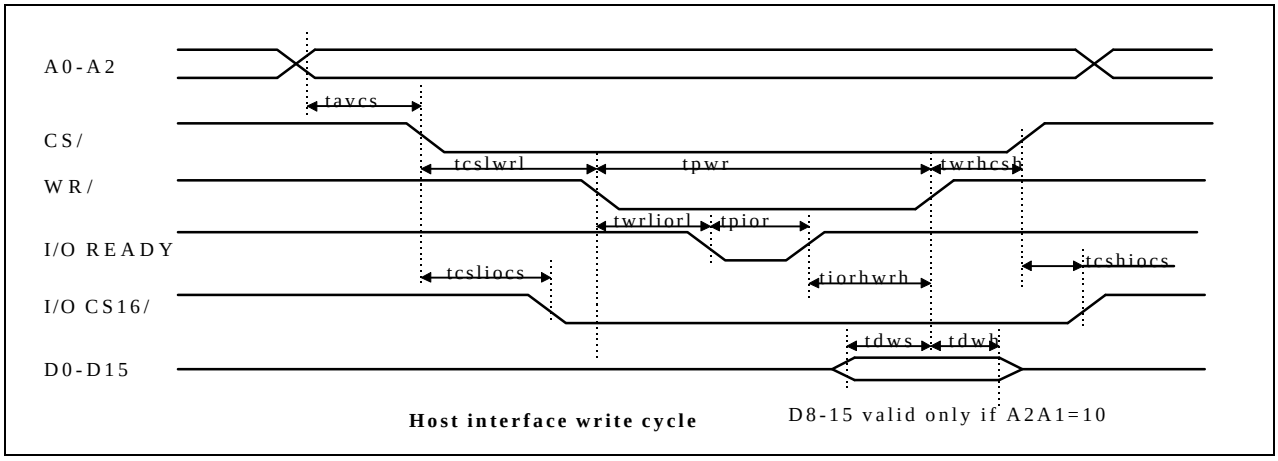
There is a trade-off between the crystal frequency and the support of widely available external DRAM/ROM components. The following chart allows to select the best fit for a given application :

Sample rate (KHz)	Xtal (MHz)	tck (ns)	ROM tA (ns)	DRAM tRAC (ns)	DRAM tRC (ns)	COMMENT
48	12.288	20.35	92	72	92	maximum frequency
44.1	11.2896	22.14	101	80	101	
37.5	**9.60**	**26.04**	**120**	**95**	**120**	**Recommended for current designs**
31.25	8.00	31.25	146	116	146	

Using 9.6 MHz crystal frequency allows to use widely available DRAMs with a cycle time tRC of 120 ns and a RAS/ access time of 95ns, as well as widely available ROMs.

7-2- PC HOST INTERFACE



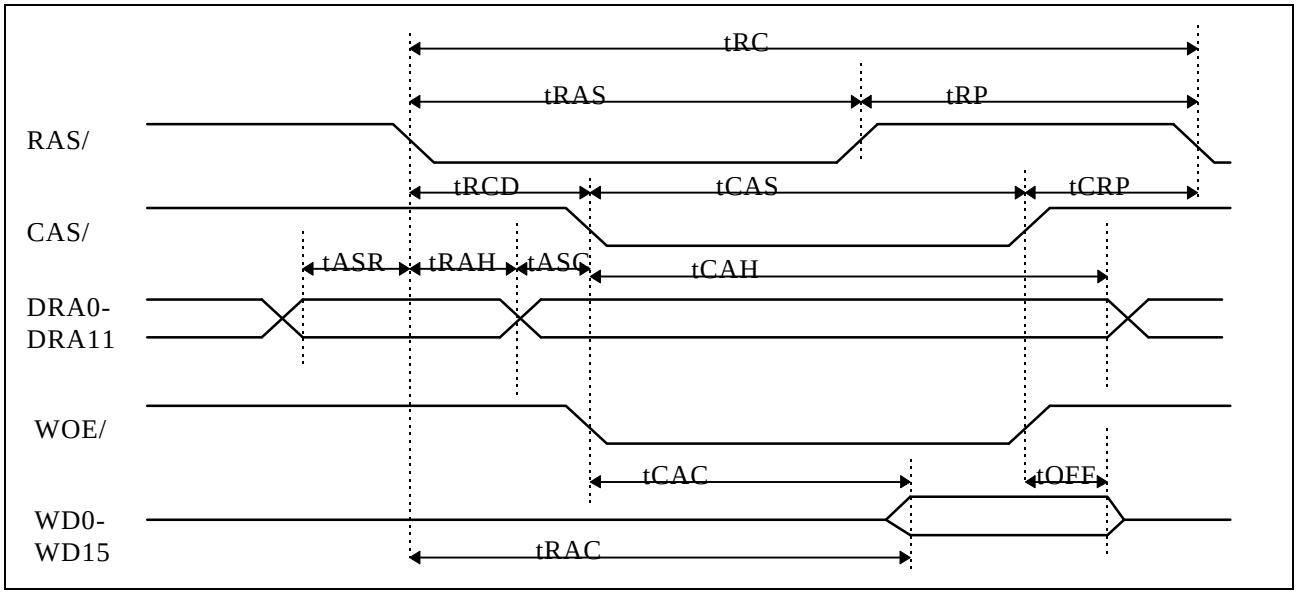


Parameter	Symbol	Min	Typ	Max	Unit
Address valid to chip select low	tavcs	0	-	-	ns
Chip select low to RD/ or SBHE/ low (note 1)	tcslrdl	5	-	-	ns
RD/ or SBHE/ high to CS/ high	trdhcsh	5	-	-	ns
RD/ or SBHE/ pulse width	tprd	50	-	-	ns
Data out valid from RD/ or SBHE/ (note 2)	trdldv	-	-	20	ns
Data out hold from RD/ or SBHE/	tdrh	5	-	10	ns
I/O ready low from RD/ or SBHE/ (note 3)	trdliorl	0	-	10	ns
I/O ready pulse width (note 3)	tpior	-	-	128	tck
I/O ready rising to data out valid (note 3)	tiorhdv		-	0	ns
I/O CS16/ low from CS/ low (note 4)	tcsliocs	0	-	20	ns
I/O CS16/ high from CS/ high (note 4)	tcshiocs	0	-	20	ns
Chip select low to WR/ low	tcslrwrl	5	-	-	ns
WR/ high to CS/ high	twrhcsh	5	-	-	ns
WR/ pulse width	tpwr	50	-	-	ns
I/O ready low from WR/ low (note 3)	twrliorl	-	-	128	tck
I/O ready high to WR/ high (note 3)	tiorhwrh	5	-	-	ns
Write data setup time	tdws	10	-	-	ns
Write data hold time	tdwh	0	-	-	ns

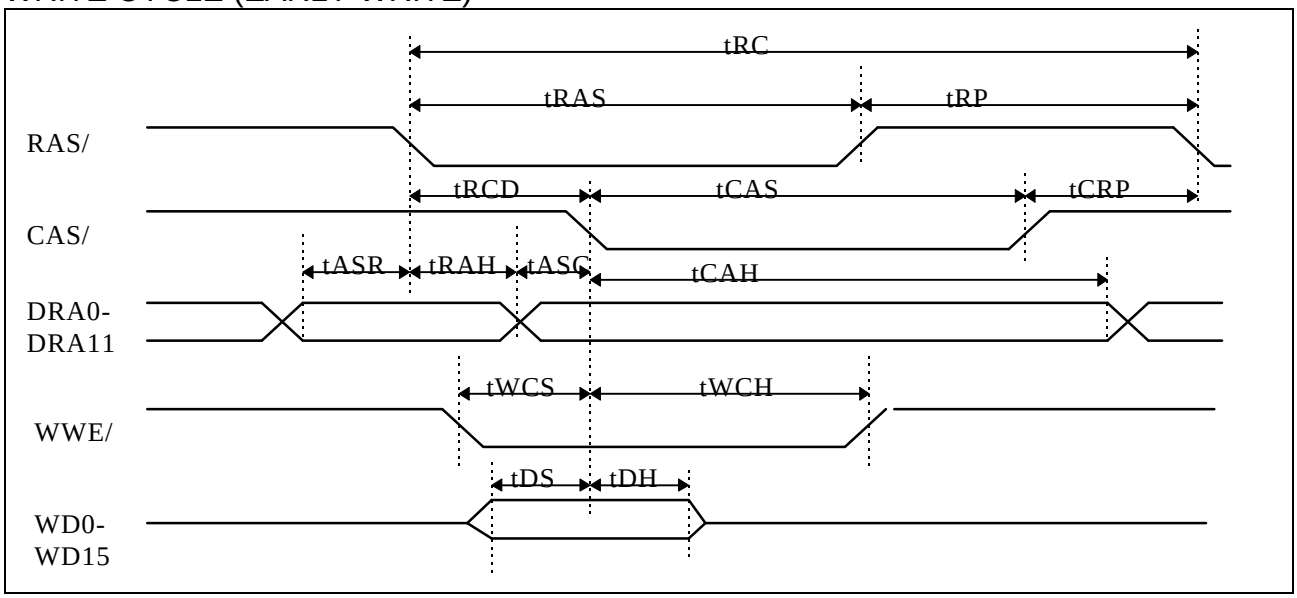
note 1 : SBHE/ is asserted by PC only if A2A1=10 (16 bits read operation).
note 2 : when data is already loaded into internal SAM9407 output register. In this case I/O READY will stay high during the read cycle.
note 3 : I/O READY will go low only if the data is not ready to be loaded into/ read from internal SAM9407 register. 128 tck corresponds to a single worst case situation. At Fck = 11.2896 MHz, I/O READY is likely to never go low when using standard ISA bus timing.
note 4 : I/O CS16/ is asserted low by SAM9407 if A2A1=10 to indicate fast 16 bits ISA bus transfer to the PC.

7-3- EXTERNAL DRAM TIMING

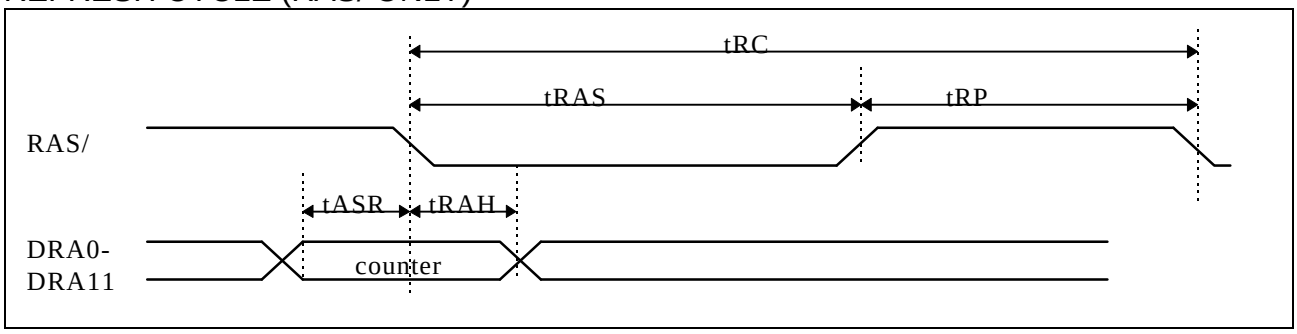
READ CYCLE



WRITE CYCLE (EARLY WRITE)



REFRESH CYCLE (RAS/ ONLY)



Parameter	Symbol	Min	Typ	Max	Unit
Read/Write/Refresh cycle	tRC	5*tck-5	-	6*tck+5	ns
Access time from RAS/	tRAC	-	-	4*tck-5	ns
Access time from CAS/	tCAC	-	-	4*tck-5	ns
CAS/ high to output Hi-Z	tOFF	-	-	2*tck-5	ns
RAS/ precharge time	tRP	2*tck	-	-	ns
RAS/ pulse width	tRAS	3*tck-5	-	-	ns
CAS/ pulse width	tCAS	3*tck-5	-	-	ns
RAS/ to CAS/ delay time	tRCD	tck-5	-	tck+5	ns
CAS/ to RAS/ precharge time	tCRP	tck-5	-	-	ns
Row address setup time	tASR	tck-5	-	-	ns
Row address hold time	tRAH	tck/2	-	-	ns
Column address setup time	tASC	tck/2-5	-	-	ns
Column address hold time	tCAH	3*tck	-	-	ns
Write command set-up time	tWCS	-	tck	-	ns
Write command hold time	tWCH	-	4*tck	-	ns
Write data set-up time	tDS	-	tck	-	ns
Write data hold time	tDH	-	3*tck	-	ns
Refresh counter average period (12 bit counter)	-	-	512*tck	-	ns

Notes :

-The multiplexed CAS/, RAS/ addressing can support memory DRAM chips up to 16 Mbits, as long as the number of row address lines and column address lines are identical. For example device type 416C1200 is supported because it is a 1Mx16 organization with 10 bit row and 10 bit column. Device type 416C1000 is not supported because it is a 1Mx16 organization with 12 bit row and 8 bit column.

-The signal WOE/ is normally not used for DRAM connection. It is represented only for reference purpose.

- As RAS/ only counter refresh method is employed, several banks of DRAMs can be connected, using simple external CAS/ decoding. Linear address lines (WAx) can be used to select between DRAM banks. For example, a 1Mx32 SIMM module may be connected as two 1Mx16 banks, with CAS0/ and CAS1/ selections issued from CAS/ and WA20.

- During a whole DRAM cycle (from RAS/ low to CAS/ rising), WCS0/ is asserted low.

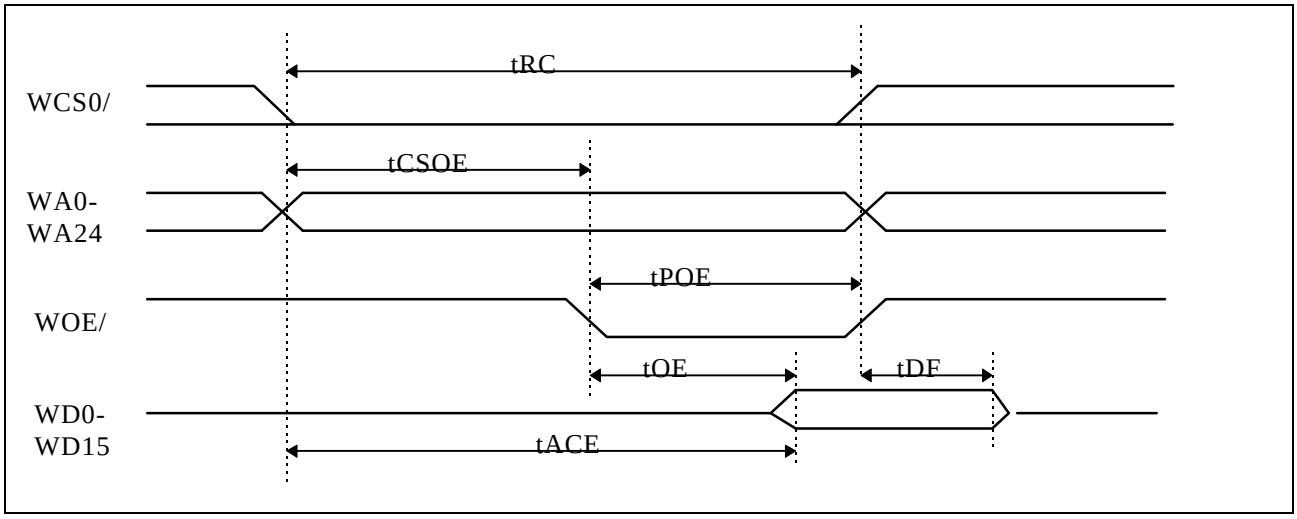
- The equivalence between multiplexed DRAM address lines (DRA0 to DRA11) and the corresponding linear addressing (WA0 to WA23) is as follows :

	DRA11	DRA10	DRA9	DRA8	DRA7	DRA6	DRA5	DRA4	DRA3	DRA2	DRA1	DRA0
RAS/ time	WA22	WA20	WA18	WA8	WA7	WA6	WA5	WA4	WA3	WA2	WA1	WA0
CAS/ time	WA23	WA21	WA19	WA17	WA16	WA15	WA14	WA13	WA12	WA11	WA10	WA9

- To save DRAM power consumption, CAS/ and RAS/ are cycled only when necessary. Therefore, depending on firmware loaded, total board power consumption may increase with synthesis processing traffic.

7-4- EXTERNAL ROM TIMING

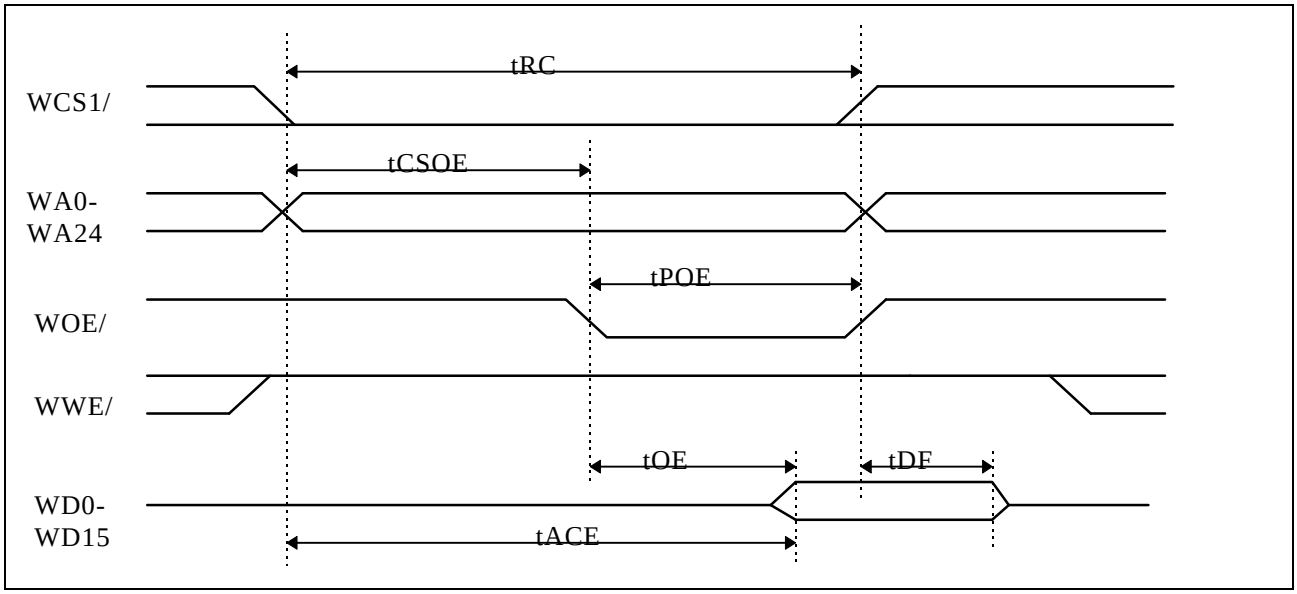
ROM READ CYCLE



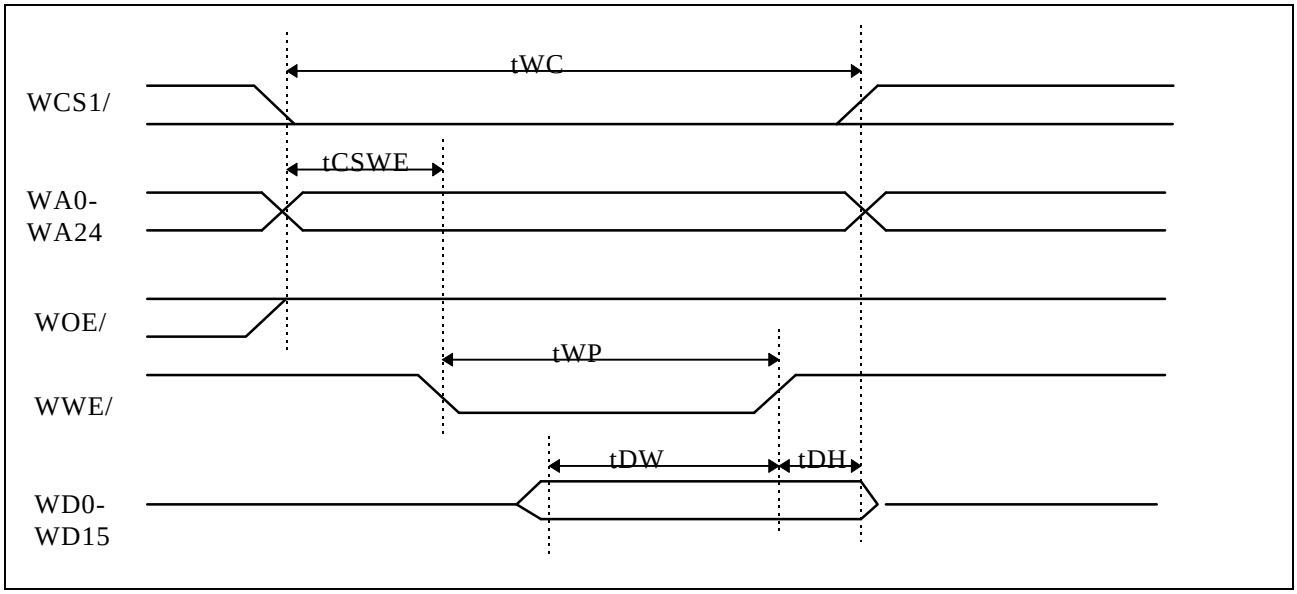
Parameter	Symbol	Min	Typ	Max	Unit
Read cycle time	tRC	5*tck	-	6*tck	ns
Chip select low / address valid to WOE/ low	tCSOE	2*tck-5	-	3*tck+5	ns
Output enable pulse width	tPOE	-	3*tck	-	ns
Chip select/address access time	tACE	5*tck-5	-	-	ns
Output enable access time	tOE	3*tck-5	-	-	ns
Chip select or WOE/ high to input data Hi-Z	tDF	0	-	2*tck-5	ns

7-5- EXTERNAL RAM TIMING

16 BIT SRAM READ CYCLE

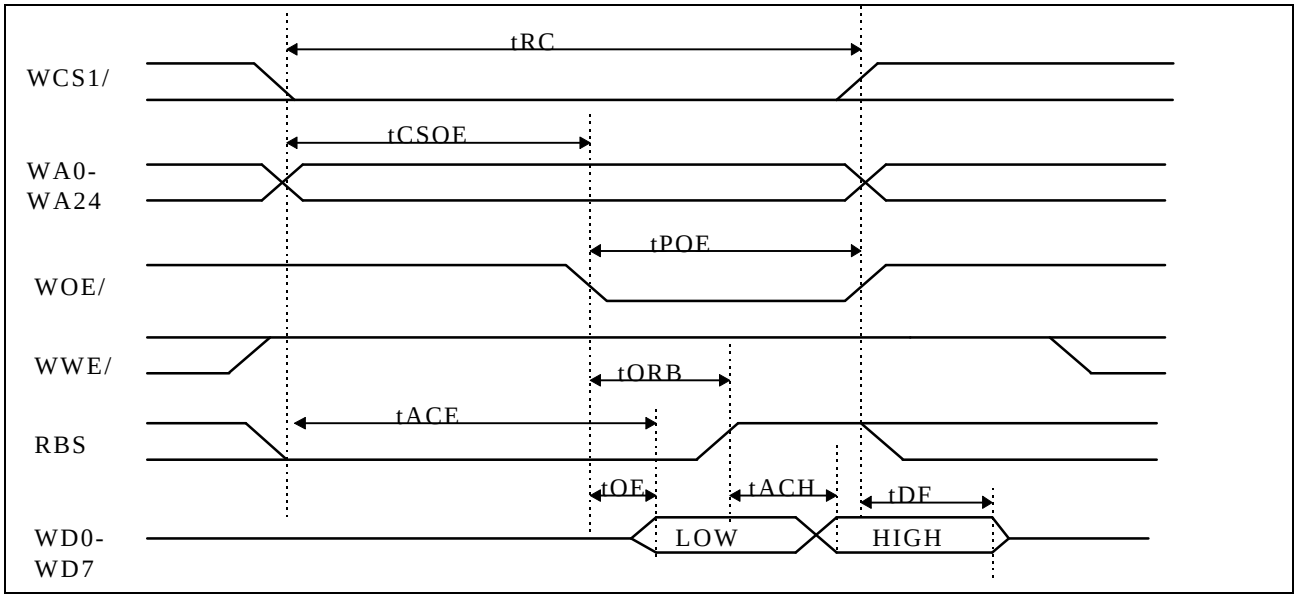


16 BIT SRAM WRITE CYCLE

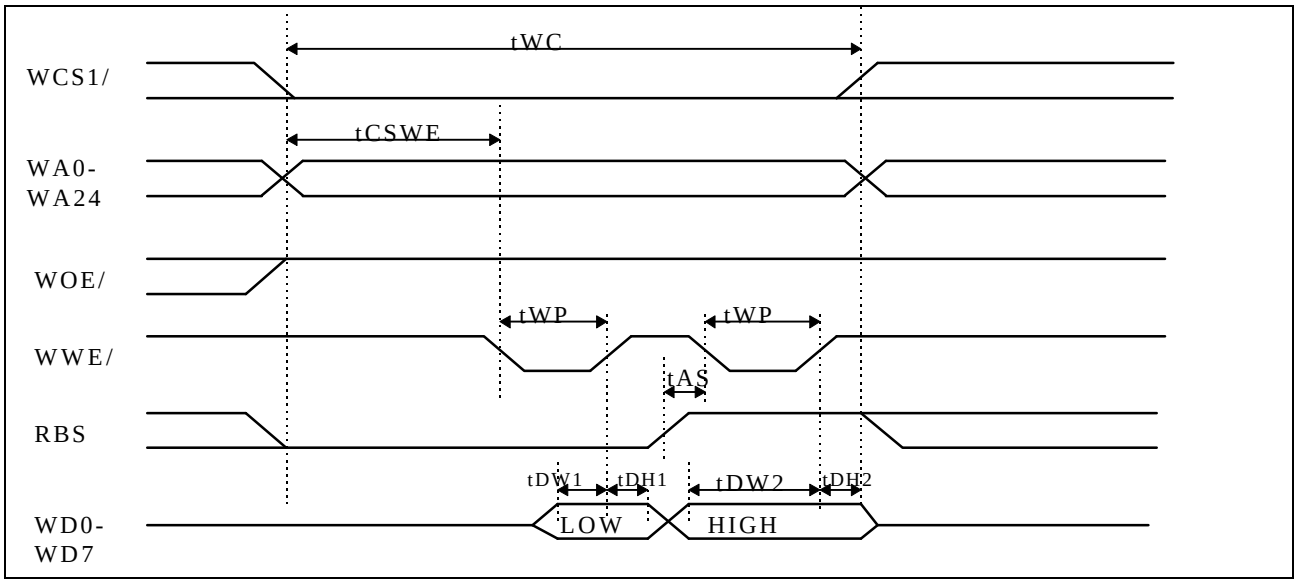


Parameter	Symbol	Min	Typ	Max	Unit
Read cycle time	tRC	5*tck	-	6*tck	ns
Chip select low / address valid to WOE/ low	tCSOE	2*tck-5	-	3*tck+5	ns
Output enable pulse width	tPOE	-	3*tck	-	ns
Chip select/address access time	tACE	5*tck-5	-	-	ns
Output enable access time	tOE	3*tck-5	-	-	ns
Chip select or WOE/ high to input data Hi-Z	tDF	0	-	2*tck-5	ns
Write cycle time	tWC	5*tck	-	6*tck	ns
Write enable low from CS/ or Address or WOE/	tCSWE	2*tck-10	-	-	ns
Write pulse width	tWP	-	4*tck	-	ns
Data out setup time	tDW	4*tck-10	-	-	ns
Data out hold time	tDH	10	-	-	ns

8 BIT SRAM READ CYCLE

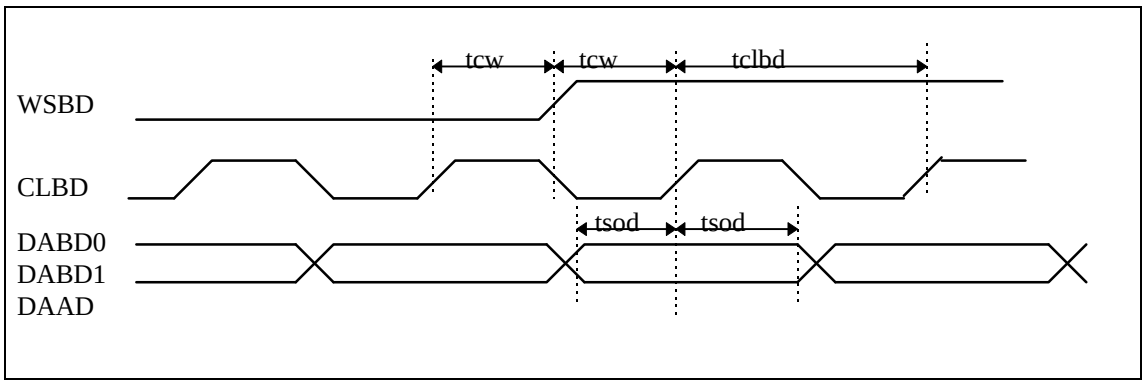


8 BIT SRAM WRITE CYCLE



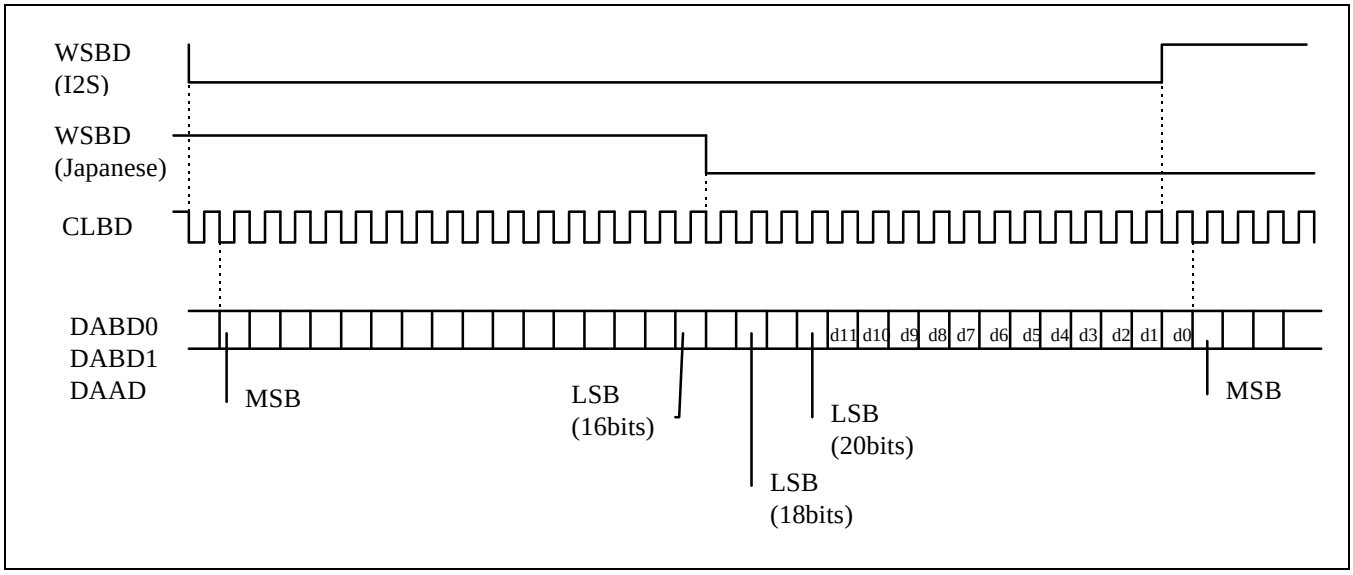
Parameter	Symbol	Min	Typ	Max	Unit
Word (2xbytes) read cycle time	tRC	5*tck	-	6*tck	ns
Chip select low / address valid to WOE/ low	tCSOE	2*tck-5	-	3*tck+5	ns
Output enable pulse width	tPOE	-	3*tck	-	ns
Chip select / address low byte access time	tACE	3*tck-5	-	-	ns
Output enable low byte access time	tOE	tck-5	-	-	ns
Output enable low to byte select high	tORB	-	tck	-	ns
Byte select high byte access time	tACH	2*tck-5	-	-	ns
Chip select or WOE/ high to input data Hi-Z	tDF	0	-	2*tck-5	ns
Word (2xbytes) write cycle time	tWC	5*tck	-	6*tck	ns
1st WWE/ low from CS/ or Address or WOE/	tCSWE	2*tck-10	-	-	ns
Write (low & high byte) pulse width	tWP	1.5*tck-5	-	-	ns
Data out low byte setup time	tDW1	1.5*tck-10	-	-	ns
Data out low byte hold time	tDH1	0.5*tck+10	-	-	ns
RBS high to second write pulse	tAS	0.5*tck-5	-	-	ns
Data out high byte setup time	tDW2	2*tck-10	-	-	ns
Data out high byte hold time	tDH2	10	-	-	ns

7-6- DIGITAL AUDIO TIMING



Parameter	Symbol	Min	Typ	Max	Unit
CLBD rising to WSBD change	tcw	8*tck-10	-	-	ns
DABD valid prior/after CLBD rising	tsod	8*tck-10	-	-	ns
CLBD cycle time	tclbd	-	16*tck	-	ns

DIGITAL AUDIO FRAME FORMAT



Notes :
- Selection between I2S and Japanese format is a firmware option
- DAAD is 16 bits only
- When connected with codecs like CS4216 or CS4218, d0-d11 can be used to hold independent auxiliary information on left and right words. Refer to corresponding Codec data sheets for details

8- RESET AND POWER DOWN

During power-up, the RESET/ input should be held low until the crystal oscillator and PLL are stabilized, which can take about 20ms. The RESET/ signal is normally derived from the PC master reset. However a typical RC/diode power-up network can also be used for some applications.
After the low to high transition of RESET/, following happens :

- The Synthesis/DSP enters an idle state, executing RAS/ only refresh cycles.
- The RUN output is set to zero.
- If BOOT is low, then P16 program execution starts from address 0100H in ROM space (WCS0/ low).
- If BOOT is high, then P16 program execution starts from address 0000H in internal bootstrap ROM space. The internal bootstrap expects to receive 256 words from the 16bit burst transfer port, which will be stored from 0100H to 01FFH into the external DRAM space. The bootstrap then resumes control at address 0100H.

If PDWN/ is asserted low, then all I/Os and outputs will be floated, the crystal oscillator and PLL will be stopped. The chip enters a deep power down sleep mode. To exit power down, PDWN/ has to be asserted high, then RESET/ applied.

9- RECOMMENDED BOARD LAYOUT

Like all HCMOS high integration ICs, following simple rules of board layout is mandatory for reliable operations :

- GND, VCC, VC3 distribution, decouplings

All GND, VCC, VC3 pins should be connected. GND + VCC planes are strongly recommended below the SAM9407. The board GND + VCC distribution should be in grid form. With current silicon releases, VC3 should be connected to VCC. Provision should be made for 3.3V VC3. The easiest way is to leave room for 2x1N4148 diodes in series between VCC and VC3.
Recommended decoupling is 0.1µF at each corner of the IC with an additional 10µFT decoupling close to the crystal.

- Crystal, LFT

The paths between the crystal, the crystal compensation capacitors, the LFT filter R-C-R and the SAM9407 should be short and shielded. The ground return from the compensation capacitors and LFT filter should be the GND plane from SAM9407.

- Busses

Parallel layout from D0-D15 and DRA0-DRA11/WD0-WD15 should be avoided. The D0-D15 bus is an asynchronous high transient current type bus. Even on short distances, it can induce pulses on DRA0-DRA11/WD0-WD15 which can corrupt address and/or data on these busses.

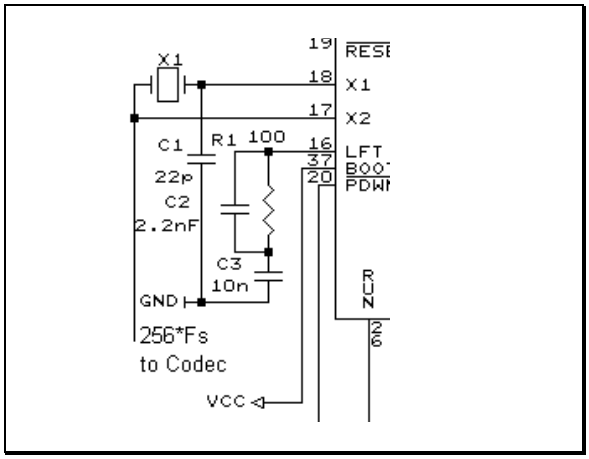
A ground plane should be implemented below the D0-D15 bus, which connects both to the PC-ISA connector and to the SAM9407 GND.

A ground plane should be implemented below the DRA0-DRA11/WD0-WD15 bus, which connects both to the DRAM SIMM grounds and to the SAM9407.

- Analog section

A specific AGND ground plane should be provided, which connects by a single trace to the GND ground. No digital signals should cross the AGND plane. Refer to the Codec vendor recommended layout for correct implementation of the analog section.

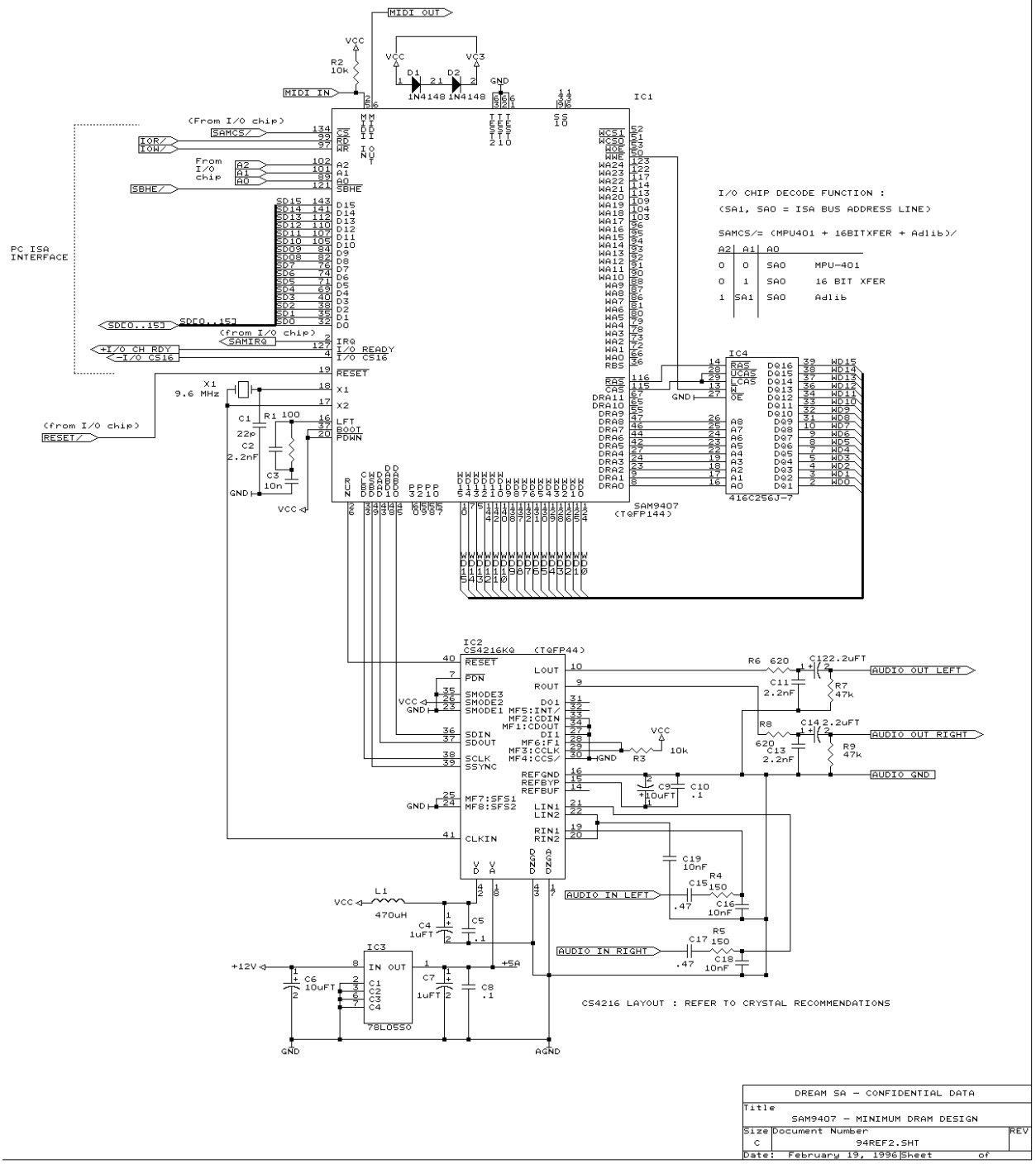
10 - RECOMMENDED CRYSTAL COMPENSATION AND LFT FILTER



Note : If the X2 output is not used as a Codec clock, then an additional 22pF capacitor from X2 to GND should be implemented.

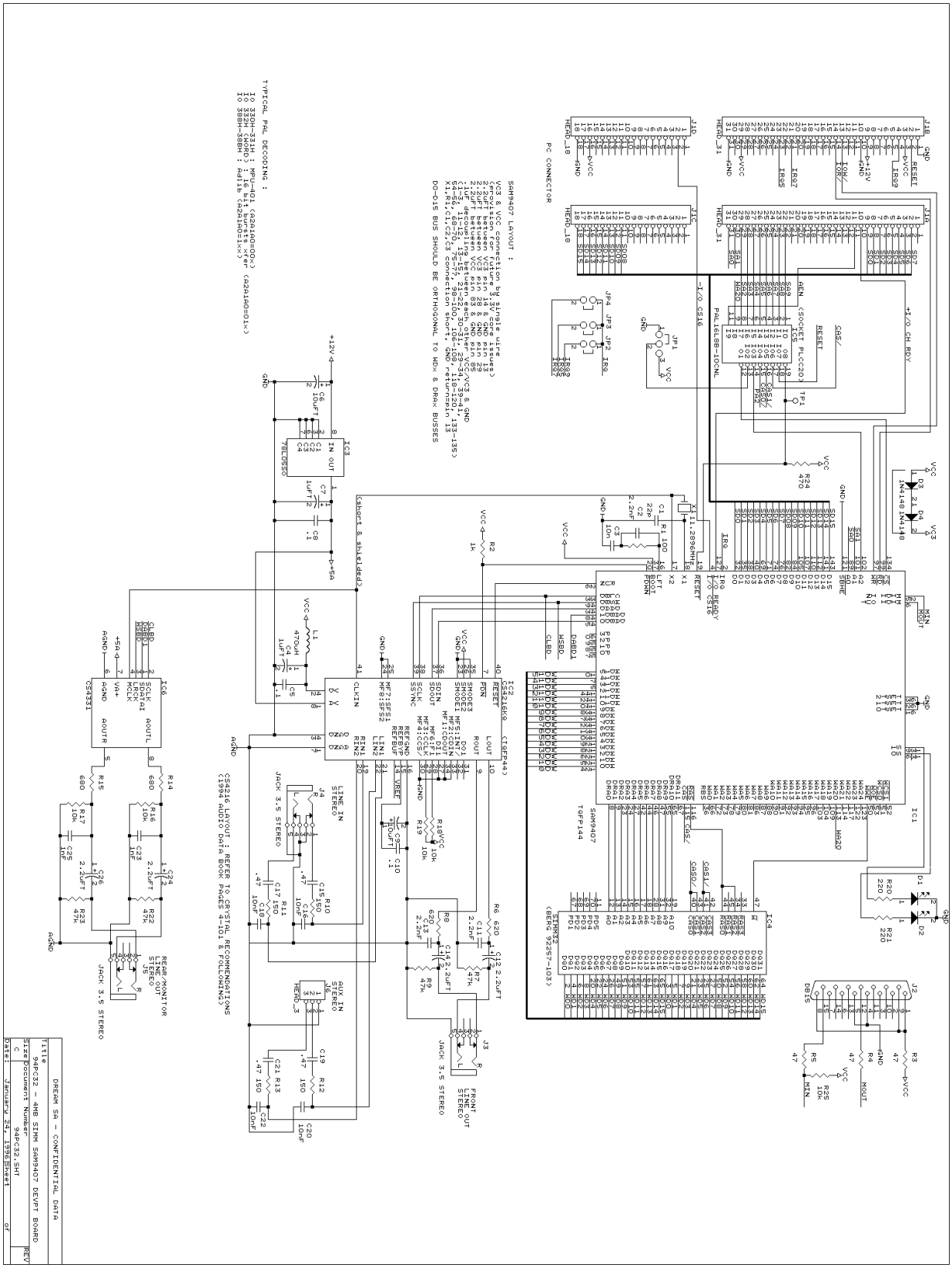
11- TYPICAL DESIGNS

11-1- MINIMUM DRAM



- √ **General Midi compliant wavetable synthesis**
- √ **Compatible reverb + chorus**
- √ **Wave play and record (one stereo channel)**
- √ **Game compatible synthesis**
- √ **3D effect**
- √ **4 bands equalizer**

11-2- COMPLETE SYSTEM USING 1Mx32 SIMM : 94PC32



NOTES :